EE Digital Electronics:

Date:	02.05.2012
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Title:	SIXIO2 UM

Introduction:

SIXIO2 is an interface module designed in FMC standard form factor. It contains two LVDS inputs, two LVDS outputs, one TTL input (terminated with 50 ohm), two TTL outputs, eight LEDs and a logic analyzer port.

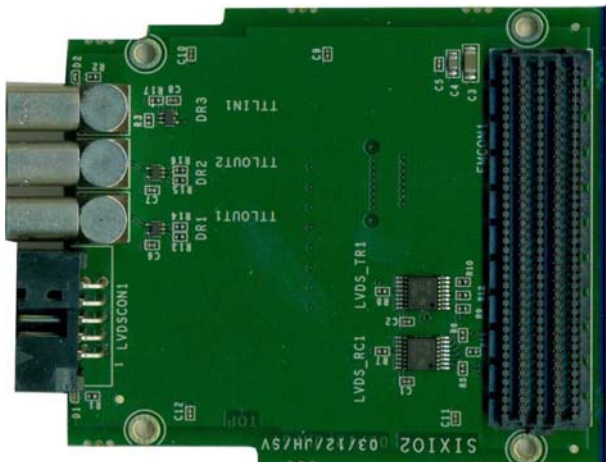

Fig. 1 Photo of SIXIO2 (bottom view)

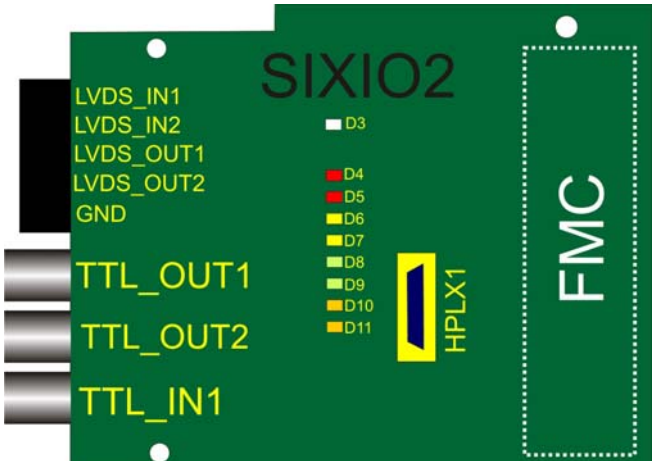

Fig. 2 Top view of SIXIO2

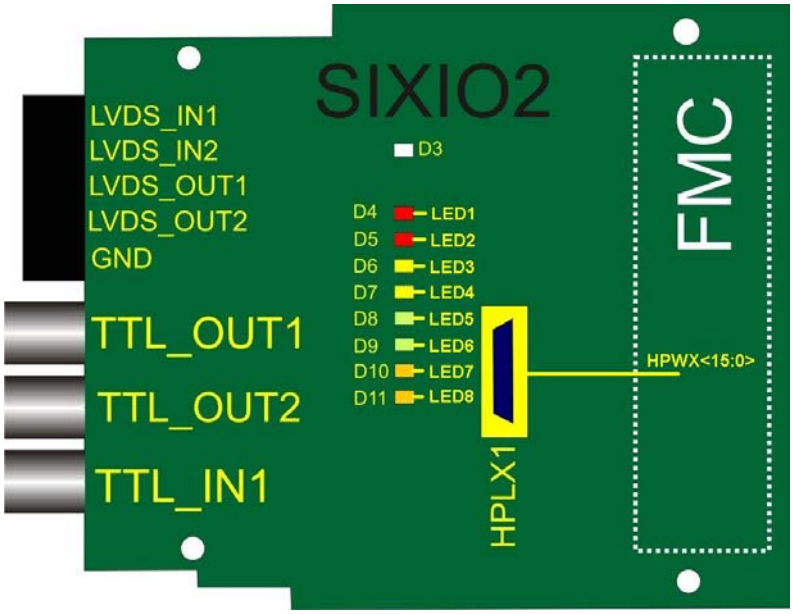

Fig. 3 Signal names of LEDs and logic analyzer port

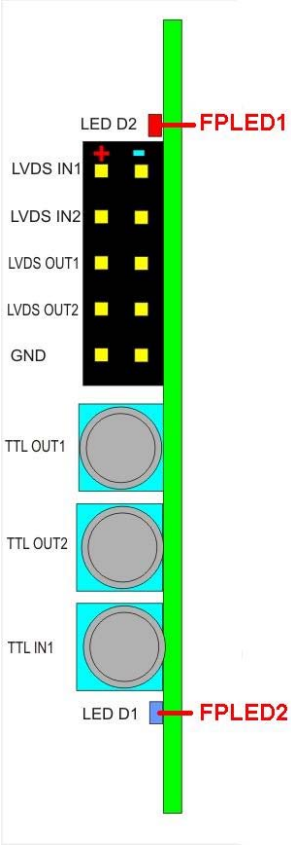

Fig. 4. Signal names of front panel LEDs

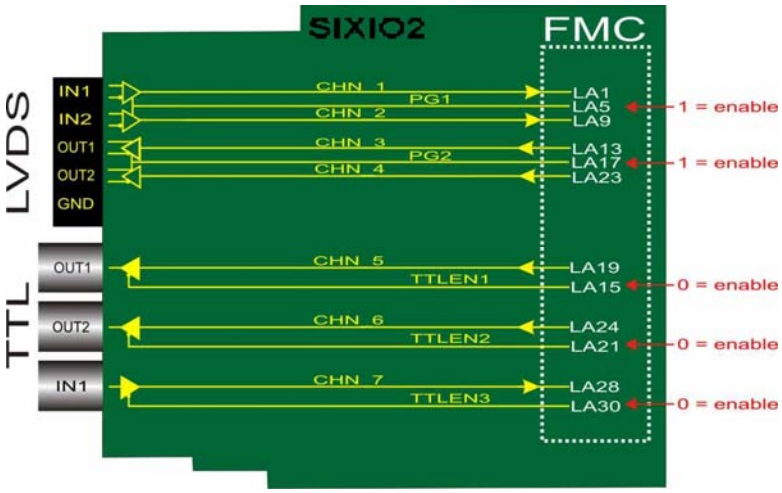

Fig. 5. Signal names of LVDS and TTL ports

Only 3.3V supply is used.

Supply current:

- Idle c.a. 6 mA.
- FPGA configured with I/O test design. 25mA.
- 125 MHz TTL output loaded with 50 ohm. 35mA.
- 200 MHz clock connected to TTL IN. 50 mA.
- 200 MHz output loaded wit 50 ohm. 60 mA.

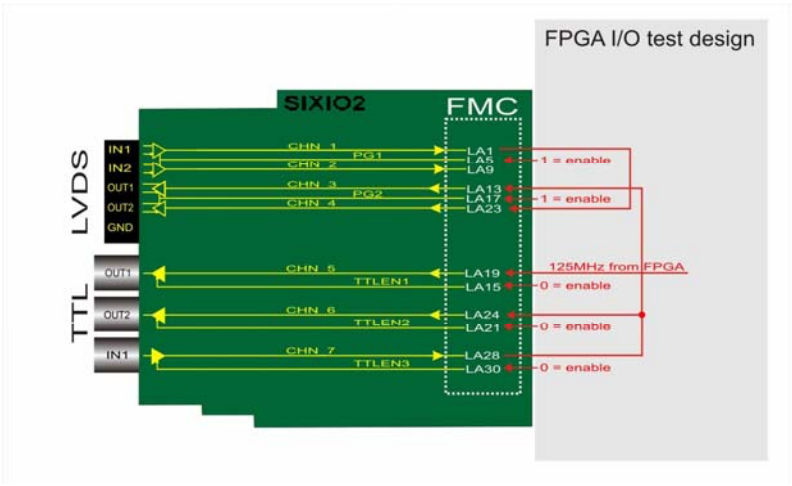

Fig. 6. FPGA I/O test design

Max frequency measured:

- 240 MHz on TTL input.
- 240 MHz on TTL output (50 ohm load).
- 240 MHz on LVDS output (100 ohm load).