Linac and Operations – Beam Instrumentation

Technical Note:

LOBI FAIR Timing Receiver Nodes Requirements 18.02.2014

Attachment to the detailed specification: F-DS-C-06e_Timing-Receivers-v3.1

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1 Contents

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2 General

The GSI department LOBI, as the main user of FAIR timing receiver modules, defines the following requirements and features for the FTRNs (Fair Timing Receiver Nodes) to be developed.

We state, that in every single DAQ system defined by LOBI, a FTRN must be installed, to ensure full access to timing and telegram information, such as timing events, beam IDs, beam processes, timestamps etc.

In general, based on the good experiences made with the CERN timing receiver modules [1], the features and functionalities of these modules should be considered for realization for the FTRNs.

See https://edms.cern.ch/document/598907/1

The technical realization within the FAIR specifications and guidelines is up to the contractor. Changes to these requirements, due to uneconomic or disproportionate efforts, may be accepted after consultation with representatives of GSI-LOBI.

We refer to the detailed specification:

F-DS-C-06e_Timing-Receivers-v3.1 from the department CSCO [2].

3 Form Factors

The following form factors for the FTRNs have to be delivered:

- VME64X
- µTCA (AMC), suitable also for Instrumentation Technology Libera System
- PCIe
- PMC
- stand-alone (1U or 2 U, 19” rack mountable, display, remote controlled (LAN))

If for any reason a priority within the production of specific form factors has to be set, GSI-LOBI requires VME, µTCA and PCIe as soon as possible. An intermediate stand-alone system (Exploder, by GSI-CSEE) is already available.

It shall be investigated, if it is possible to keep all relevant electronic trigger and synchronisation lines on all form factors equal in length to gain equal retention times, also in mixed set-ups, like VME with µTCA.

4 Properties, Logic and Use Cases

The main purposes of all FTRNs are to decode the White Rabbit timing signals/protocols to produce interrupts for FESA real-time (RT) actions and/or to generate signals on the output connectors. In addition, dedicated inputs (ext. connectors) on the FTRN front panel must be provided for external trigger sources besides the GMT events delivered by WR, to be used to create IRQs on the bus, to be sent out again on front-panel output connectors and to start/stop internal counters (see 4.1).

4.1 PTMS / Counters

Currently GSI-LOBI FESA classes make heavy use of the Peripheral Timing Events (PTMS) of the CERN Timing Receiver (CTR) [1]. A **similar** functionality is required for the FTRNs. In general, PTMS have the following main characteristics:

- programmable trigger source (GMT events, external input,…)
- programmable output (IRQ on bus and/or signals on output connectors)
- programmable output delay (8 ns – few seconds)
- programmable output width (8 ns – few seconds)
- programmable mode (run once, multiple, burst, continous)
- programmable logic level (norm./inverted out)

Example: In the CERN CTR module these features are realized by loading a counter with the programmed values on reception of the trigger. The output is triggered when the counter reaches 0. Additional functionality for the counters includes self-start with next clock cycle.

The GSI CSCO-TG group uses macros to create pulses, delays, bursts and clocks, which is appreciated. As output clocks/frequencies are most often used for tests and diagnosis, not all possible frequencies must be realized. A large selection of even and common frequencies in different order of magnitudes (0.1 Hz up to 10 MHz) is sufficient.

Use cases:

- On a GMT event an instantaneous pulse is released, either on the bus or front panel output connector, or both. The latency between event and pulse release must be constant, known and as short as possible.

- Generation of one or more programmable external clock signals for DAQ electronics, bursts and pulses. Used for the SIS Fast Current Transformer: generate multiple triggers per machine event for multi-event ADC to acquire bunch data every N-th revolution.

- Chained operation (example: next counter starts, when previous counter finishes) to be used as:

    1. increased delay or gate operation (example: counter provides signal output when started until it reaches 0).

    2. programmable, machine event based gates for ADCs.

    3. dedicated sequences of sampling clocks: e. g. 2 s at 100 Hz Clock, then a 2 MHz Burst for 100 ms, then again 100 Hz for 3 s, and this in a loop or only once, or started by software, or by GMT events or ext. trigger, synchronized either with external or internal clock.

See also Figures 1 – 4 for some basic examples of output pulses.

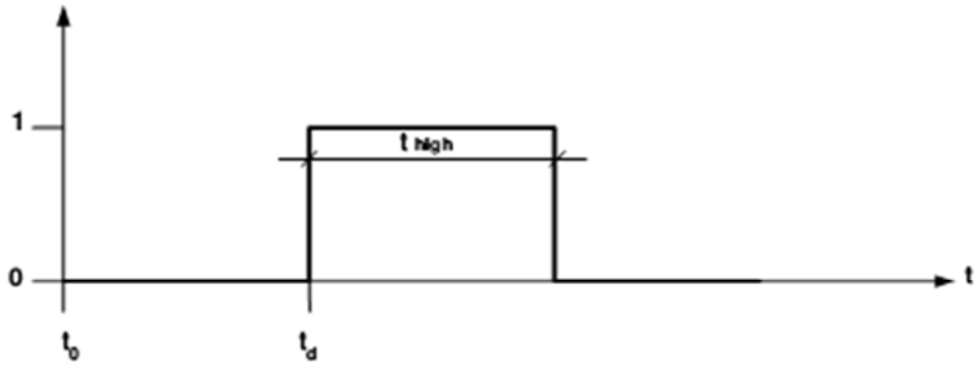

Figure 1: Single Gate: The event defines the reference point in time t_0. After the delay time t_d has elapsed, a single pulse of length t_{high} is released on the respective channel. This pulse forms a gate with a defined length of $t_{high.}$ For the duration of t_{high} the signal is switched into *active* state.

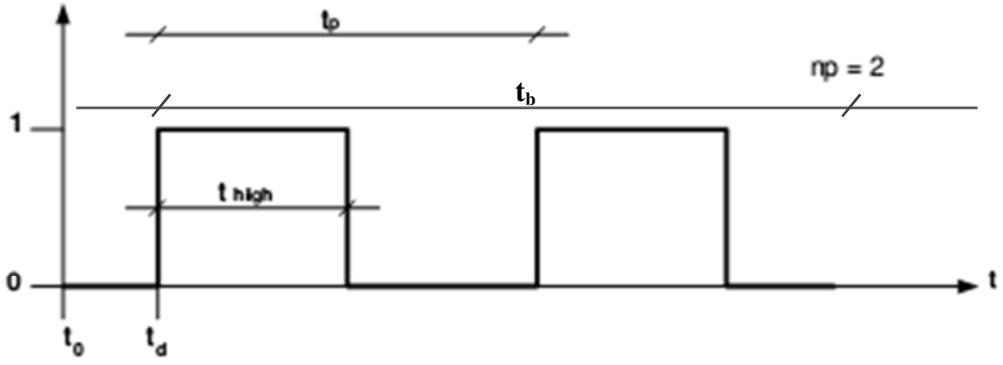

Figure 2: Single Burst: The event defines the reference point in time t_0. After the delay time t_d has elapsed, a pulse of length t_{high} is released repeatedly on the respective channel. The period length is defined by t_p. The number of cycles can either be determined by the two parameters number of pulses np or burst duration t_b. For the duration of t_{high} the signal is switched into *active* state.

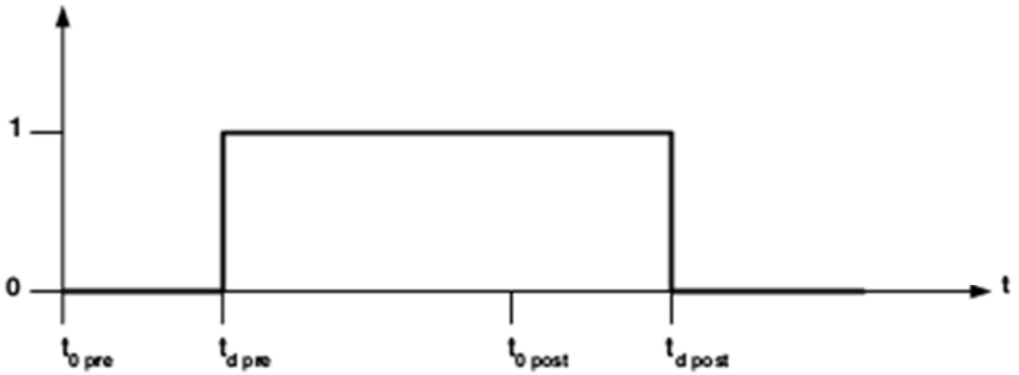

Figure 3: Toggling Gate: A pre-event defines the reference point in time t_{0pre}. After the first delay time t_{dpre} has elapsed, a one-time static signal is released on the respective channel. A post-event defines the reference point in time t_{0post}. After the sceond delay time t_{dpost} has elapsed, an inverted static signal is again transmitted to the respective channel. Hence, the duration of the trigger gate is defined by the time interval between the two events (incl. the consideration of the respective delay times). The signal is switched into the state *active* during t_{high} defined by t_{dpre} and t_{dpost}. A cyclic operation is not foreseen.

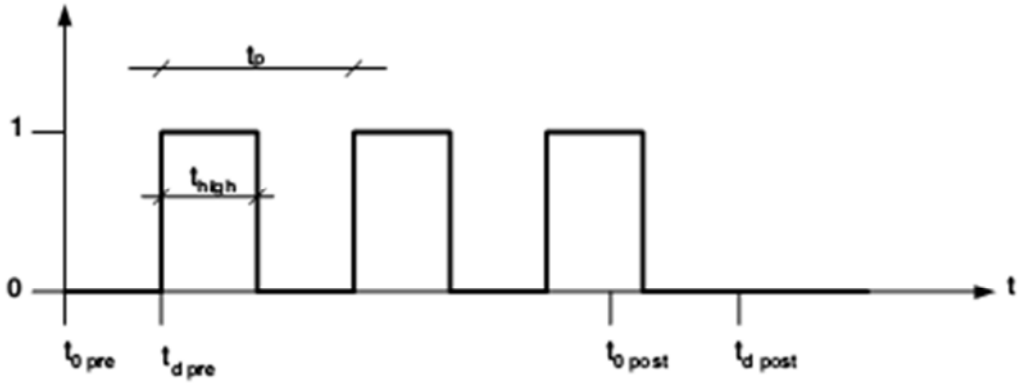

Figure 4: Toggling Burst: A pre-event defines the reference point in time t_{0pre}. After the first delay time t_{dpre} has elapsed, cyclic pulses of duration t_{high} are repeated on the respective channel. The period length is defined by t_p. A post-event defines the reference point in time t_{0post}. After the second delay time t_{dpost} has elapsed, the output of the cyclic pulses is terminated. The output duration of the cyclic trigger gate is defined by the time interval between the two events (incl. the consideration of the respective delay times). Commencing with the start of the first cyclic pulse, the output signal is switched alternately into the states *active* or *inactive*.

4.2 Rate Divider

It should be investigated, if a rate divider function can be implemented.

1. A real rate divider creating a fraction of a frequency (External pulse in -> divided rate on front panel output and/or IRQ generation)
2. Reduction of a number of cycles or events (with or without a dedicated beam/beam process/Virt. Acc) delivered by GMT and being used on front-panel and/or as bus IRQ to trigger RT actions. The foreseen use case is data reduction.

4.3 Coincidence

Programmable standard logic (AND/OR/NOT) on at least two of the external inputs should be provided.

5 Software

All software must be available as source code. The software must be developed for Linux i686 (Scientific Linux 6 or later) and must be provided for 32 and 64 Bit OS.

It is expected, that at least two Linux drivers for the PCI (PCIe, PMC, µTCA) and VME (VME64X) based systems are delivered. In addition, full integration into the FESA environment is a must, including the denotation of timing events (e.g. #32 = Cycle Start).

A test and configuration tool for all hardware features (from user point of view) must be provided. The ctrtest [1] program from CERN may be used as an example. Starting this stand-alone tool with a script file (as parameter) may allow for automated configuration of the FTRN e.g. at boot time. In addition, this test software allows to observe and display the timing itself, e.g. history of events, payloads, telegrams.

To access the FTRN hardware, a FESA class using a driver or API, and based on the latest FESA Version at GSI, is required. This FESA class allows programming the settings of the FTRN, e.g. clock out, on the front-end, either manually, by LSA or at boot-time. In addition, this FESA class is required for monitoring the FTRN. All user relevant properties must be available for get, set and subscription.

Simple tools (operational on the FEC for testing) shall visualize the beam cycles, the local CPU/FTRN clock, and the available timing infos in general.

A firmware update shall be as easy as possible for the untrained user, best by usage of dedicated software to upload the firmware file.

All software must be delivered with source code and documentation.

Item No.	**Feature/Function**	**Remarks**
1	Module driver	I686, X86_64, Linux with RT patch (32/64 Bit)
2	Test- and configuration software	Linux, C/C++, full access to module and timing
3	FESA Class	full access to module and timing
4	Timing Library	
5	Simple tools	Show machine super cycles/interrupts/events/time

5.1 LAN Timing System

GSI-LOBI suggests installing an Intranet LAN-Timing, based on the actual WR machine timing to operate and test timing based DAQ systems, **also where WR is not available**. This could also be used to synchronize applications over the LAN. A reduced precision is accepted.

6 Hardware

6.1 I/O Ports

Dependent on the available front panel area of the respective form factor, the following in- and outputs (Lemo), besides the WR SFP cage, are required:

- Pulse/Clock Out (min. 3), programmable invertible logic
- External Trig. In (min. 2), programmable logic
- Ref Clock In (>0 – 50 MHz)*
- Ring RF In for the µTCA FTRN
- LEDs for status and activity, general and for all connectors

* can be skipped, if an alternative sync mechanism using a stand-alone WR switch is feasible.

For the time being, it is assumed, that all front panel connetors can be used as in- and output after configuration.

6.2 Signal Level / Trigger

Pulse levels shall be TTL or LVTTL. It should be possible to invert the logic by user settings. Open inputs shall be pulled up to high state. Default trigger on positive slope.

6.3 Special Requirements

It must be possible to host and operate one or more modular FTRNs per host crate at a time.

µTCA Timing Receiver for the BPM System in SIS100:

All BPM Libera ADC sample clocks shall be synchronized. This can be done by a sync signal delivered by WR and locked by a PLL on the FTRN. An internal creation of a 250 MHz clock is required to be distributed on the µTCA backplane to the ADCs in the Libera. It must be guaranteed, that all samples of all up to 16 ADCs per Libera can be correlated/synchronized within the 4 ns granularity.

In addition an external clock IN is required to sync the ADCs with external signals. This Ext. Clock In shall accept a 10 MHz sinusodial signal. The FTRN locks to this signal and creates the 250 MHz (max.) on the Libera backplane. This clock IN can be **skipped**, if a stand-alone WR switch is able to accept an external

reference sync clock to be locked on a WR compatible output and to be connected to the FTRN via fiber optical link to its SFP port.

Important: An input is required to insert ring RF for bunch detection purposes in BPM systems. This signal must be distributed to the connected FPGAs on the ADC boards.

µTCA Timing Receiver for the BPM System at pLinac:

The 4 Libera systems for the 14 beam position monitors of the proton linac should have the capability of sampling all 16 ADC boards synchronized to the 325.224 MHz Linac Master Oscillator, which is available from a distributed external rf signal source. The Master Oscillator is linked to a PLL/logic to create a low jitter, phase aligned ADC sample frequency of 118.2632727 MHz (=Master Oscillator * 4/11). This sampling clock shall be distributed via the backplane to all ADC cards. This dedicated frequency must not concern the general FTRN FPGA logic, which is not able to generate such frequencies.

One solution could be a piggy board or AMC module on top of the FTRN which allows for switching between the internally generated ADC clock and the 325.224 MHz ADC clock derived from the external Linac Master Oscillator signal. An appropriate programmable on-board circuitry (switching) for this frequency range is required.

The Linac Master Oscillator signal must not be introduced via the FTRN front-panel, but rather via the available space of the unused GDX slot in the Libera systems. An SMA connector on a front-panel mounted on the unused slot is suggested. A short coaxial cable from the SMA to the MCX or MMCX connector on the FTRN board links external oscillator signal and PLL.

NB: It is quite clear, that this requirement does not perfectly fit to a standard timing receiver board. Optional it is possible to create the 118.2632727 MHz in an external electronic device and feed this signal to an additional input on the ADC boards e.g. with already matched line length to the ADCs.

Stand-Alone Timing Receiver:

The stand-alone system shall be easily configured to generate simple tasks such as start and stop trigger immediately. A reset button shall be installed to switch back to a default state. The accelerator operational concepts to define possible filters such as beam process, events, beam IDs are not known so far. The functions of this stand-alone FTRN shall have access to these filters with simple switches or turn keys or touch pad/ display with knobs to create or extract any event at any time of the ACC cycle (event plus delay). All settings and activities shall be visible via front-panel display and LEDs at the output connectors. The system shall be fully remote-controllable. Programming via USB with e.g. Notebook/PC is ok, but not sufficient, programming via LAN must be foreseen.

A GUI (e.g. Java) is required to readout, show and list all configurations and presets.

Switching between local and remote operation of the stand-alone timing receiver must be done in hardware (button or switch). The actual status of local or remote operation must be displayed in the GUI. There must not be a timeout

after which the timing receiver switches to remote operation automatically. The set operation mode „local/remote" of the timing receiver must be a property which can be read remotely.

Fan In/Out Option:

It shall be investigated, if a digital Fan In/Out logic can be implemented. An external signal shall be multiplied and sent out to selected or to all outputs. This is used to trigger/latch ADC or Scaler modules in the systems nearby or inside the host crate.

This feature is used to replace FAN In/Out modules of other form factors (e.g. NIM) and could save significant costs.

The external reference clocks (either via WR switch or by ext. Sync IN, if required) shall be also locked with the fan logic as well. This, to lock the signal to internal counters and to provide an external signal for diagnosis (e.g. oscilloscope).

6.4 Specification Table

No.	Feature	Value	Remarks
I/Os			
1	Number of Trigger Inputs	min. 2	Best case: all connectors can be used as in- and outputs
2	Number of Outputs	3 - 8	Dependent on form factor
3	Active State	high or low active	Programmable
4	Logic Level	LVTTL	
5	Input Impedance	High impedance (TTL std.) or 50 Ω	Cf. section 7 Note: A display/readout for the type of termination is desirable.
6	Output Impedance	50 Ω	
7	Connector Type	Lemo 00 female	
Reference Clock In (Front Panel): **to be skipped in case of operational WR switch synchronisation. The stated parameter must apply also for the switch based synchronisation.**			
8	Number of Ref. Clock Inputs	1 - 2	Second input for 5V TTL pulse can be evaluated
9	Bandwidth	0 – 50 MHz	
10	Signal Shape	Sinusoidal	For pulse wave (5V TTL) a switch or second Ref. Clock In can be evaluated

11	Input Impedance	50 Ω	
12	Signal Level	-10 dBm – +20 dBm	
13	Connector Type	Lemo 00 female	Or good alternatives (tbd)
pLinac Reference Clock In (Only µTCA FTRN)			
14	Number of Inputs	1	For master rf signal
15	Number of Outputs	Not defined	Distribution to all ADC modules
16	Input frequency	325.224 MHz	
17	Output frequency	118.263272 MHz	4/11 of master rf; to be used as ADC sample clock
18	Input Signal Shape	Sinusoidal	
19	Input Signal Level	< 10 dBm	
20	Input Impedance	50 Ω	
21	VSWR	< 1.2	
22	Front pannel connector type	SMA female	
Clock Fan Out Backplane and Front (opt.) (µTCA/Libera)			
23	Jitter	<+/-200 ps	
24	Precision	< 1 ns	
25	Max. frequency	250 MHz	
Fan In/Out Front Panel (all FTRN)			
26	Number of Inputs	1	
27	Number of Outputs	All available outputs	
28	Logic Level	LVTTL	
29	Bandwidth	0 – 50 MHz	
30	Ratio	1:1	
31	Propagation Delay	<10 ns	
Activity LEDs			
32	Module OK	1	
33	WR-Status (On, Link, Lock, PPS)	4	Active, if connection to WR is established. (Definition by CSCO-TG)
34	I/O Direction	1 per I/O	Red coloured. Active, when used as output.
35	I/O Activity	1 per I/O	Rising edge active
36	Ref. Clock In	1	Only, if dedicated ref input is

			realized. Active, if a valid clock signal is fed in.
37	Bus Access	1	Active, if there is a READ/WRITE/Interrupt access
38	IRQ	1	Active, if FTRN activates an interrupt request line
39	Enabled	1	Active, if timing decoder is enabled
VME			
40	Standard	VITA VME 64X	Hot plug, handles, P1/2 with 5 rows, outer rows not used, P0 prepared, but not assembled (not required today)

7 Use cases for digital in/outputs

Remark: It should be investigated, if it is possible that inputs may be converted on a reprogrammable way to outputs and vice versa to gain I/O flexibility.

In any case we need:

1. External Inputs: this input reacts on external pulses to trigger an interrupt (e.g. a FESA Realtime Action, Custom Event Source). The minimum number of inputs is two (Start, Stop).

2. With two external inputs a logic unit for all possible logic functions (AND, OR etc.) can be implemented to trigger an IRQ and/or to generate a pulse on the front panel output.

3. Sources delivering 3.3V TTL or 5V TTL signal with an output impedance of 50 Ω or lower are connected to the inputs.

4. An external input signal may be processed by a rate divider:
    a. directly logic clock/pulses in, also randomly distributed, and a fraction being released on an output connector
    b. a rate division for dedicated multiplexed (beam process or Virt Acc based) events from the timing system (eg for data reduction)

5. External Clock Input (Ref Clock): either to be used to synchronize (or replace) the internal clocks (counters) or the ADC sampling via the FTRN (e.g. in µTCA for Liberas only, 250 MHz). Max input freq: 50 MHz This input can be skipped, if an alternative way of external synchroniztaion via e.g. a WR switch, is feasible.

6. Two types of signal termination connected to the outputs are possible:
    a. High input impedance
    b. 50 Ω input impedance

7. Stand-Alone: 19", 1 or 2 U, preset timings are accepted, display, switches and knobs for settings, Network Interface, In- and Outputs, LEDs, like all FTRN. Local and remote reset.

8 IRQ Handling

A „Queue On" command saves IRQs with timestamp in a queue for seq. processing. „Queue Off" dismisses the IRQ. IRQ handling is not in the scope of the users. It must be assured, that either all IRQs are used/registered or some are dismissed on user decision. Default should be „Queue on".

It must be possible to channel the IRQ to the bus, to the front panel output or both.

9 References

[1] The CTR User Guide, https://edms.cern.ch/document/598907/1

[2] F-DS-C-06e_Timing-Receivers-v3.1