White Rabbit Technology as Basis for the FAIR Timing System

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The FAIR timing system has the task of triggering and synchronizing equipment actions as required by the parallel execution of different beam production chains. It must handle machine cycles from 20 ms up to several hours for storage rings. Although a precision of 1 µs is sufficient in most cases, some equipment like kickers needs timing with nanosecond precision. For synchronization of radio-frequency components, the timing system is complemented and linked to the Bunch phase Timing System BuTiS [1], but this is out of the scope of this document.

White Rabbit

The advent of the FAIR facility requires inevitable changes for the accelerator timing system due to larger distances and the need for higher precision. Furthermore, open technology shall be applied that is used by other major research facilities as well. A new timing system for FAIR will be based on a White Rabbit (WR) network [2,3]. WR is a protocol being developed further by CERN, GSI and other partners for synchronizing nodes in a packet-based network. It combines Gigabit-Ethernet, IEEE1588-2008 (PTP), precise knowledge of the link delay and Synchronous Ethernet: Time synchronization is achieved by adjusting the clock phase (125 MHz carrier) and offset (Coordinated Universal Time - UTC, or International Atomic Time - TAI) of all network nodes to that of a common grandmaster clock. It has been demonstrated, that sub-nanosecond synchronization with a jitter in the picoseconds range is achieved over distances of a few kilometers and across dedicated WR network switches.

Equipment action will no longer be directly triggered upon receiving signals from a central timing unit. Instead, timing systems using WR networks are based on the notion of absolute time. Like alarm clocks, timing receivers (TR) in a WR network are pre-programmed for autonomous execution of actions at a given date and time. Thus, distribution of information through the network and timely execution of actions are decoupled.

Complementary Building Blocks

Network. TRs are programmed to execute actions at a given time via so-called timing-events, which are broadcasted from a central master using UDP or raw Ethernet with high priority. The network must be deterministic with known upper bound latency, such that timing events are not received too late. Since packets are transmitted without handshake and may be lost, Forward Error Correction techniques such as Reed-Solomon encoding are required. Redundant links will be used at the critical parts of the timing network [4].

Etherbone (EB) is a network protocol layer meant for fast, low level communication. It connects two distant Wishbone System-on-Chip buses and provides direct memory access to network devices [5]. EB shall be deployed at WR nodes at FAIR and CERN and its use includes transmission of timing events.

Soft-CPU. WR firmware includes a small "Soft-CPU" for reusing existing open source software. This approach saves development time and FPGA area. At GSI, the LM32 from Lattice is now used in several designs for low-priority tasks, but also serves for debugging attached Wishbone devices [5].

Status and Outlook

In 2011, White Rabbit has been established as the basis for the FAIR timing system and significant progress was made on essential building blocks. This allowed detailed specification of form factors for FAIR Timing Receivers, PSP code 2.14.10.3.3. Further work included porting WR firmware from Xilinx to Altera FPGAs, the latter being used by TRs developed at GSI. The distribution of time stamps with WR has been successfully shown. The focus in the near future is on the integration of different building blocks. This is required for broadcasting timing events and demonstrating the capability of triggering synchronized actions. The authors would like to thank the "White Rabbits" at CERN for support and collaboration.

References

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