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|  – Technical Note | | Nr.: 20100510 (orig. mom_Nr.: 20090506) |
| Integration and Linking between FAIR Timing System and BuTiS result of meetings on 07.10.2009 and 18.11.2009 | | Author: T. Fleck |
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| Meeting | Integration / Linking between FAIR Timing System and BuTiS |
| Goal | Definition of Interfaces and Design Decisions |
| Agenda | TOP 1: System Description and System Behaviour TOP 2: Design Decision / Interface Definition TOP 3: Miscellaneous |

| TOP 1 System Description and System Behaviour | | | | | |
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| 1.1 | I | FAIR Timing System / White Rabbit | | | |

The FAIR timing network is based on synchronous ethernet and PTP (precision time protocol) using GbE (gigabit ethernet) and special layer 2 switches, so-called "white rabbit (WR)" switches. It will be carried out in tree topology where one global system timing master broadcasts all FAIR/GSI events campus-wide to up to 2000 timing event receivers (TRs).

WR protocol and WR switch specification are a result of a collaboration between different institutes and companies, mainly CERN and GSI, to fulfil all necessary requirements for control system usage – especially determinism and time accuracy. Timing events (so-called special "high priority (HP)" ethernet frames) will have deterministic maximum switch latency times and all nodes (TRs) are synchronised with the timing master to an absolute time (UTC correlated) with an accuracy in the low ns range.

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Connections between switches will be realised in fibre optics while connections between the last switch and most event receivers will either be conducted with standard ethernet twisted pair copper cables using RJ45 connectors or also in fibre optics.

Altogether the signal propagation time from the timing master to the most distant node is <~15 μs: signal propagation time ~10 μs for 2 km fibre length, ~500 ns for 100 m copper cable, WR switch latency equals 64 Byte (512 ns on GbE) for HP packets, up to four layers of switches used.

The timing master broadcasts a series of telegrams containing events about every 100 μs at the beginning of each so-called "granularity window" (its size not fixed yet, but will be a multiple of 10 μs).

Each event stream consists of a header and several events; its possible content is shown in Figure1.

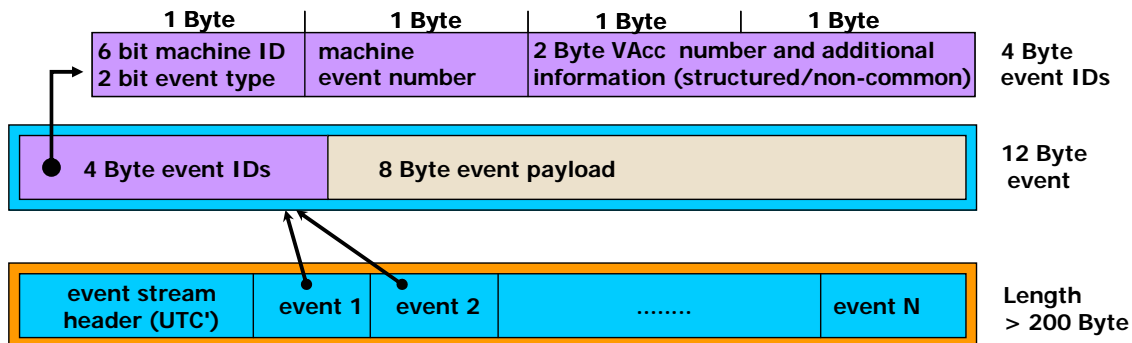


Figure 1: Timing system event streams. The shown event layout is not yet definite regarding event size and event content.

Every single event contains the information about its exact execution time (absolute or relative, but this will be totally transparent to the user). Preferably each event is sent in the granularity window preceding the event execution time. "Empty" event streams will be sent and used as e.g. heartbeats for all TRs in cases where no real machine events for the next granularity window exist.

Since no event loss can be accepted, some special implementation of forward error correction is used. Therefore each event stream consists of several encoded network packets.

In principle it is also possible within the timing system's event streams to broadcast additional information received from dedicated TRs.

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| 1.2 | I | BuTiS | | | |
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The Bunchphase-Timing-System BuTiS is a campus wide elaborated clock synchronization and distribution system as needed for all FAIR RF components. It distributes a 100 kHz ident clock, a 10 MHz reference clock, and a 200 MHz clock - optionally derived from a GPS receiver.

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All RF receivers are phase matched to each other with a jitter in the sub-ns-range but have a delay δt to the original clock due to individual path lengths.

A small deliberate phase shift will be introduced to the 100 kHz clock ticks to identify a defined 200 MHz clock period, the phase reference period. The frequency of both clocks is of high stability.

The corrected time reference with sub-ns precision is the positive zero crossing of the 200 MHz clock while the 100 kHz ident clock T_0 is used to unambiguously identify the otherwise periodic 200 MHz clock ticks.

The delay correction δt is in the order of 5 μs and is defined by the longest signal path propagation time from the BuTiS master to any BuTiS receiver. In the local Reference Synthesizer, synchronized to the received 10 MHz and 100 kHz signals, the delay δt is compensated for a 100 kHz T_0 and the 200 MHz clock signal C2.

It will only change if the signal distribution time itself changes due to e.g. temperature effects on the transmitting fibres and its change will stay well below 1 μs throughout the year.

| TOP 2 Design Decision / Interface Definition | | | | |
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| 2.1 | D | Usage of UTC in the Timing System, Clock Domain Problem, Accuracy Requirements | | |

Clock domain problems / UTC usage

Timing receivers connected to RF DDS cards have to create events and set values with a well-defined reference (phase) to T_0 . To achieve this, the following technical solution will be implemented:

- i) The timing master receives the time corrected 100 kHz T_0 clock (and also the 200 MHz clock on the same link) from a “BuTiS Local Reference Synthesizer”.
- ii) The timing master synthesizes the 100 kHz T_0 clock and broadcasts so-called “tuning words” throughout the WR timing system as additional event stream content – the repetition rate of the transmission is not fixed yet and will be defined from accuracy requirements and stability of the two clocks used (BuTiS / GPS).
- iii) WR timing receiver cards are able to locally reproduce (re-synthesize) the original 100 kHz T_0 clock with high accuracy regarding frequency and phase (most probably this feature will only be implemented in the SCU).

The timing master itself will be connected to some GPS (or Galileo) UTC receiver and deduce a master clock for the whole timing and control system from that input.

In Figure 2 the correlation between the timing system and BuTiS is illustrated.

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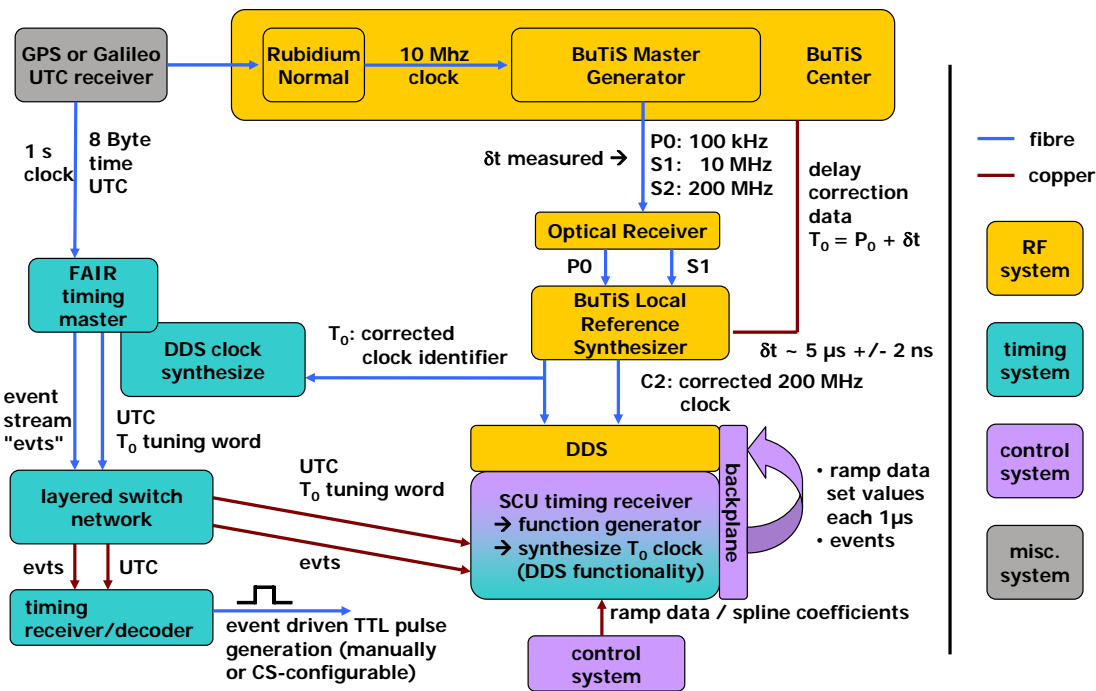


Figure 2: Correlation between RF BuTiS system and FAIR timing system.

Accuracy requirements, RF ramp data generation

Timing accuracy requirements to the control systems set values and events for the RF systems are relaxed with respect to inter-RF requirements since high precision BuTiS clocks will be used for synchronized set value generation of individual RF interface cards in different crates.

Design decision and requirements to the control system are listed below while related problems/flaws are discussed in 3.1:

It has been agreed that only for RF DDS application the function generator ("FG") will be run on the SCUs FPGA, which is not appreciated by the controls electronics group but accepted for the time being. While the SCU bus backplane allows data communication of four to five 16-bit transfers per μs, two are needed for one 24-bit value as needed for RF frequency ramp set values. Since the FG will generate ramp set values at 1 MHz, only one DDS card is supported.

RF ramps will not immediately be started by an event. Instead the SCU starts writing ramp set values as soon as the according event (e.g. "ramp start") is valid, however not immediately: Ramp start will be delayed since the first ramp set value should not be communicated one μs before and after a T₀ clock tick as described below. The DDS card receives set values and implements a buffer of at least 10 values.

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The SCU starts writing ramp data in an allowed window of $\{T_0 + 1 \mu\text{s} \dots T_0 + 9 \mu\text{s}\}$. This ensures that the first set value has a distance of at least $1 \mu\text{s}$ from any $100 \text{ kHz } T_0$ clock tick as illustrated in Figure 3. As soon as a DDS card receives set values they are written into a set value buffer and from the first 200 MHz clock tick after the next T_0 tick on, those data are executed each μs (FIFO) – provided that the $100 \text{ kHz } T_0$ clock runs with the exact frequency of 100 kHz . With this mechanism the high synchronicity of different DDS cards is realized.

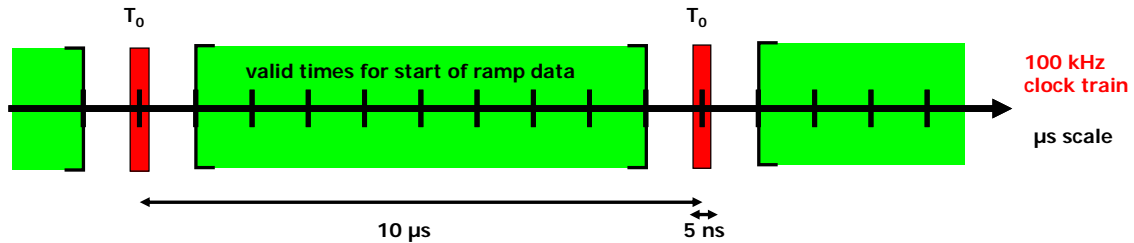


Figure 3: Valid times to start setting ramp data with respect to individual T_0 clock ticks. The BuTiS T_0 clock ticks have a high time of 5 ns .

Since ramps will have lengths of up to about 100 s both clocks in the SCU (resynthesized BuTiS) and in the DDS card (original BuTiS) have to be highly stable and synchronized in frequency since the set value buffer (size 10) must never over- or underrun.

A direct result of this design decision is that during ramp execution no other communication between SCU and DDS card is possible!

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| TOP 3 Miscellaneous | | | | |
| 3.1 | I | Design Flaws and Restrictions | | |

Description:

There are several flaws and possible problems regarding the solution specified within this document that have been addressed, discussed and specified in the meeting and will be shortly described in this section. The reason for all of them is the decision that the function generator will be run on the SCU's FPGA and not on each DDS's FPGA as had been specified in former documents.

The reason for the agreement to host the FG on the SCU is that the DDS FPGA has limited resources (about 5000 logic elements) where a huge percentage of them is already used (the FG needs about 500 logic elements).

Most of the DDS cards needed for FAIR have already been produced (about 60). An evaluation of the RF group searching for pin compatible FPGAs with more logic elements unfortunately yielded no results.

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However it was agreed that if it should be necessary, out of technical reasons, to redesign/revise the RF board design, this will be done using a more powerful FPGA and the FG will then be hosted on the RF DDS cards. This would naturally dissolve restrictions in ramp start times (as discussed in 2.1 together with Figure 3) and allow for communication during ramp execution.

Flaws and Problems:

All ramp set values have to be transmitted via SCU bus backplane where only one 24-bit set value can be transmitted per μs to only one slave card where one value per μs is needed¹.

Problems:

- 1) In the proposed solution the SCU is only aware of one slave card while the others listen to ramp data send to this card. It would be favourable to address all cards individually to have status read back and to assure proper bus communication. This however is not possible if all ramp data have to distribute via the SCU bus backplane.
- 2) It would be much easier to only execute a ramp start event via the SCU bus backplane in-between two real RF T_0 pulses. In the specified solution ramp data for up to about 100 seconds have to be transmitted with 1MHz on the SCU bus backplane where no buffer over- or underrun is allowed using a buffer size of 10 on the DDS FPGA and two different clock domains on DDS and SCU. Therefore higher requirements to synchronization and BuTiS clock synthesis within the SCU are to be met ($\pm 0.5 \mu\text{s}$ in 100 s).
- 3) During ramp execution no other communication between SCU and DDS card is possible!
- 4) One important result of the functionality described here is that all RF action can only start at the same time as a T_0 clock tick while other devices (like the ACU interfaced magnet power supplies) can have arbitrary ramp execution start times. Therefore a jitter between ramp execution of e.g. magnets and cavities of up to $10 \mu\text{s}$ will occur.

¹ Four to five 16-bit words per μs where two are needed for a 24-bit word.