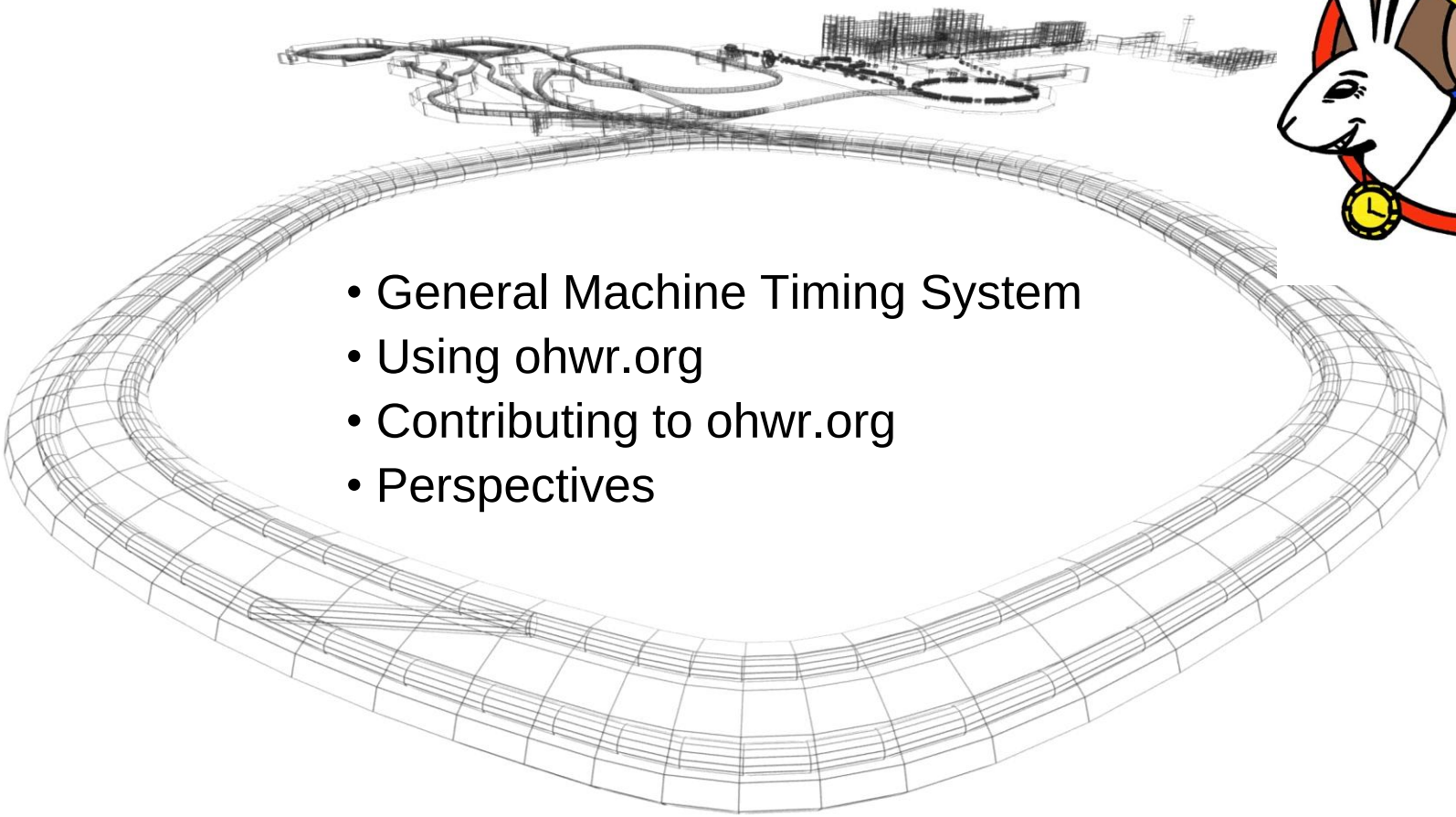
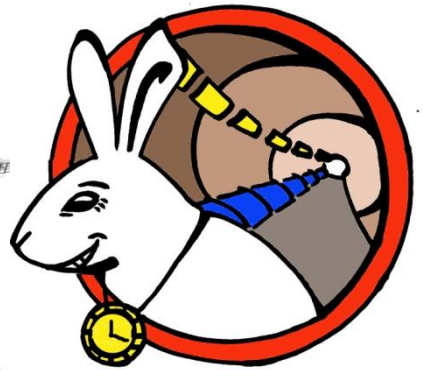
Experience and Perspectives of Open Hardware “at GSI”



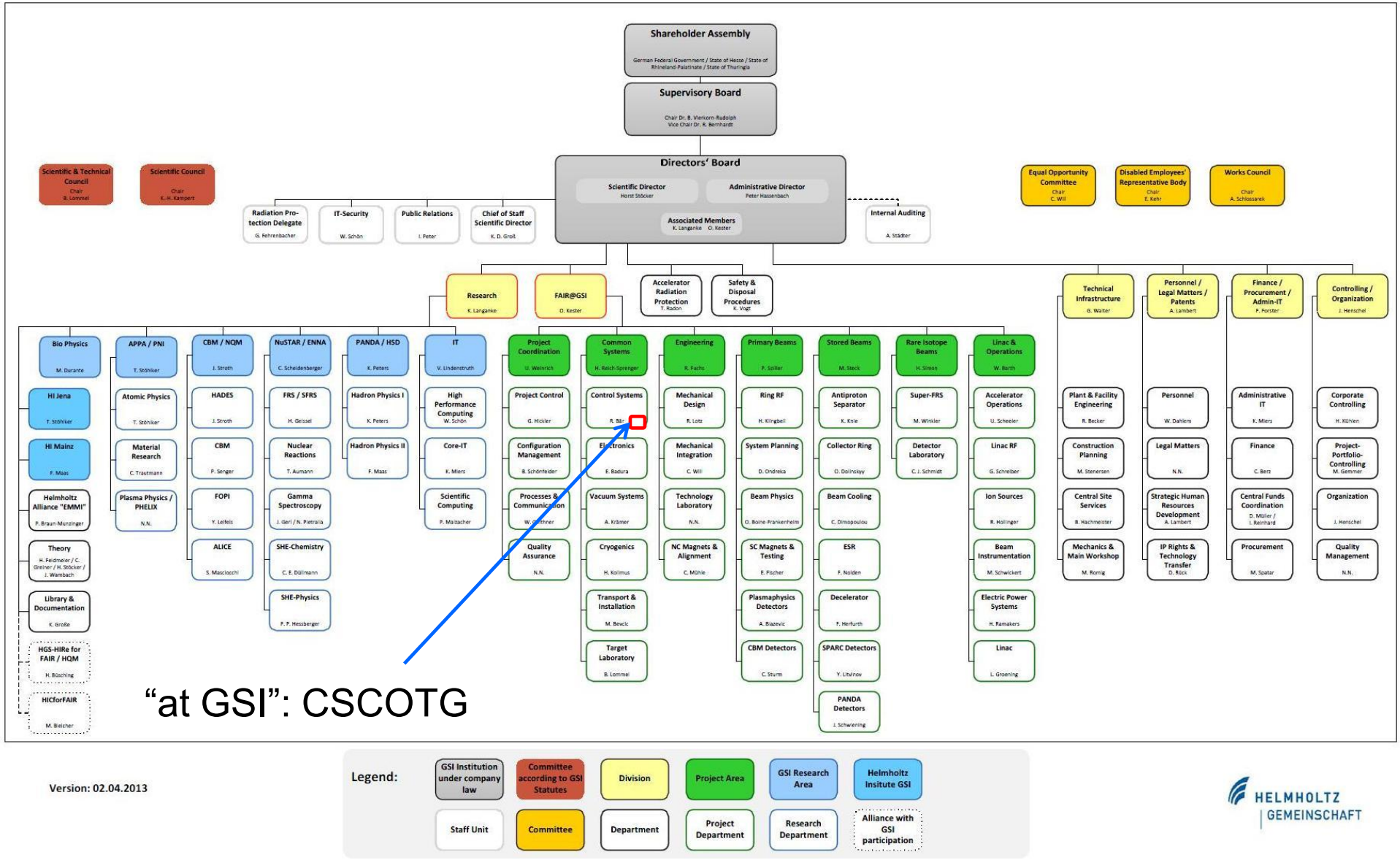


- General Machine Timing System
- Using ohwr.org
- Contributing to ohwr.org
- Perspectives

Acknowledgements

- GSI Timing Team: Marcus Zweig, Stefan Rauch, Mathias Kreider, Cesar Prados, Wesley Terpstra, Ralph Bär, Dietrich Beck
- CERN Timing Team: Tomasz Włostowski, Javier Serrano, Maciej Lipinski, Evangelia Gousiou, Erik van der Bij, Jean-Claude Bau, Pablo Alvarez, Greg Daniluk, …
- GSI/EE: Jan Hoffmann, Nikolaus Kurz, Holger Brand, …
- ...

Organization Chart



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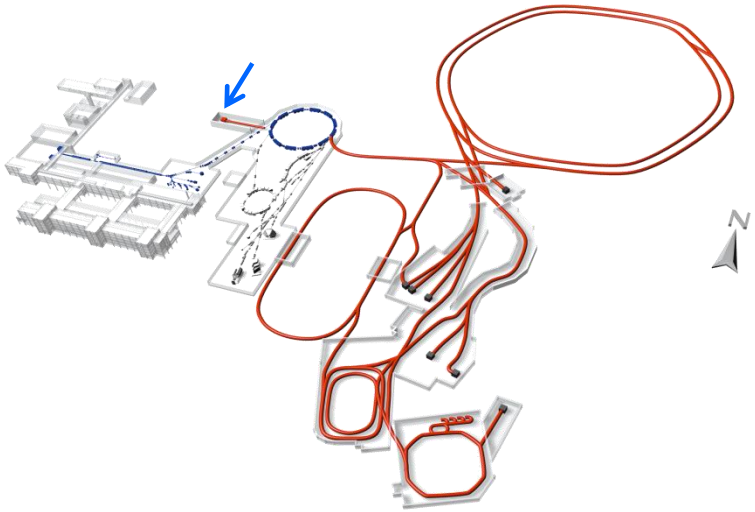
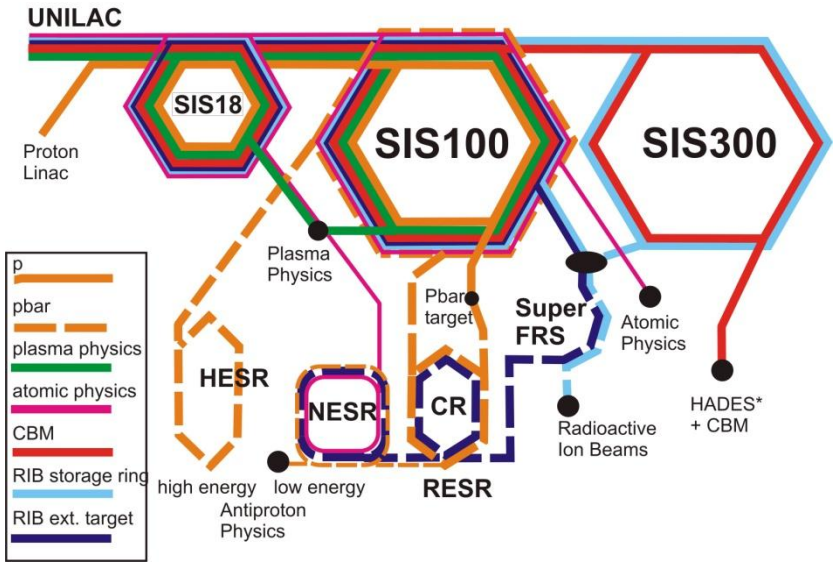
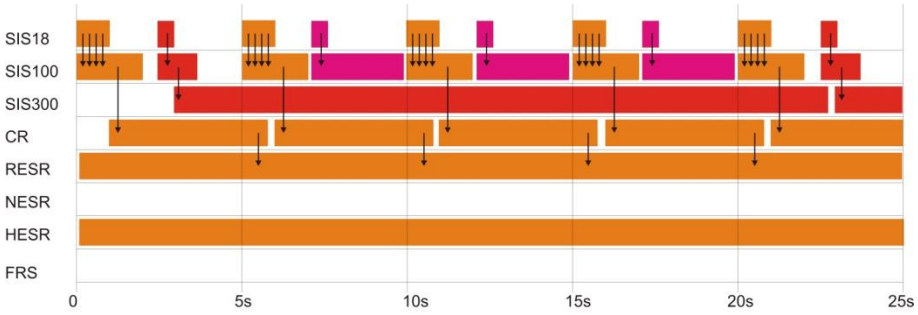
HELMHOLTZ GEMEINSCHAFT

General Machine Timing System @ FAIR
Based on White Rabbit PTP (WR, ohwr.org)



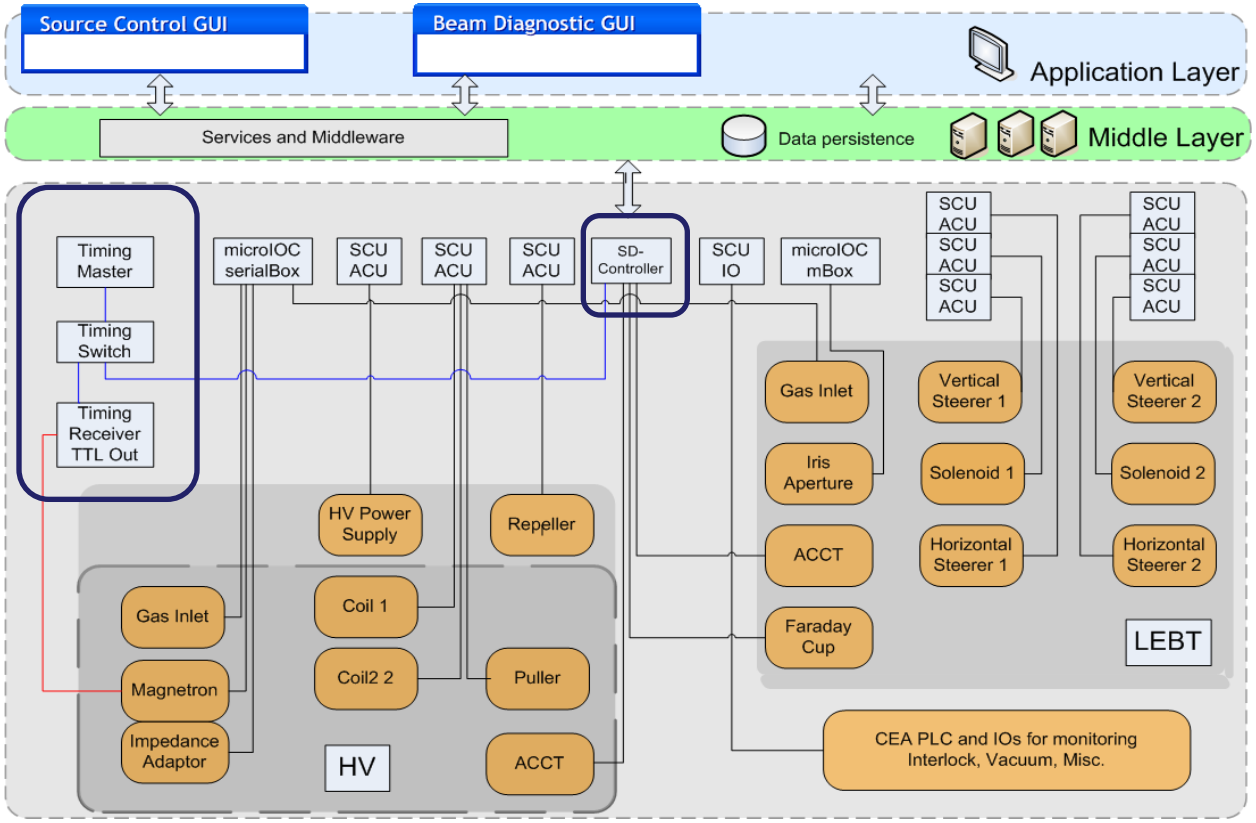


- parallel execution of beam production chains
- cycles: 20ms to hours
- trigger and sync. equipment actions
- 1 µs precision in 99% of all cases
- few ns precision for kickers
- (few ps for rf-systems: BuTiS)
- many rings
- > 2000 devices connected to timing system
- large distances
- robustness: lose at most one timing-message per year



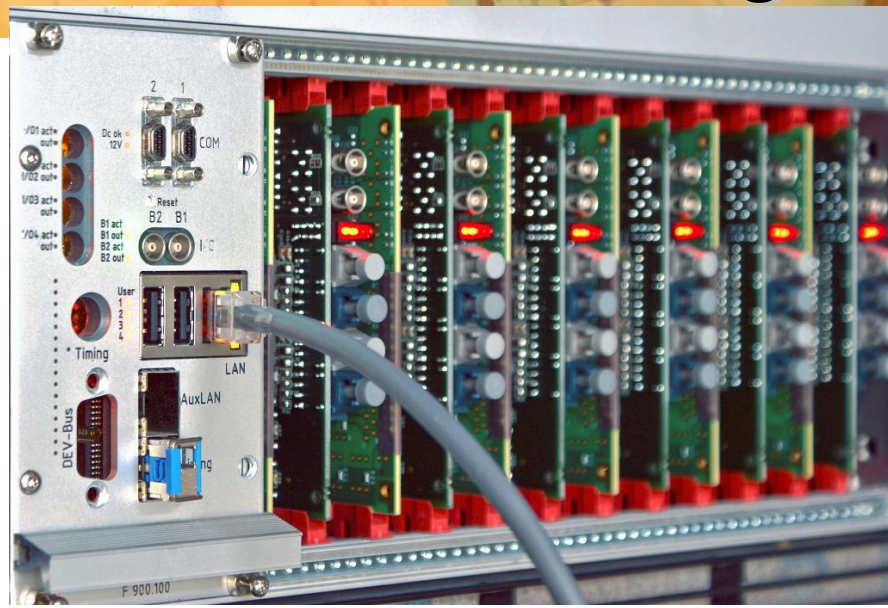
Operation Mode #5: pbar in HESR, CBM in SIS300 and high energy Atomic Physics.

Milestone R1: Timing System for pLinac Source "A Very Sophisticated 4 Hz Pulse Generator"



- first operational timing system - "simple pulse generator"
- standalone operation
- timing master, 2x timing receiver, timing switch
- milestone achieved!
- shipping to Saclay in November 2013

Timing Receiver Nodes – Different Approach than ohwr.org



SCU (Scalable Control Unit)

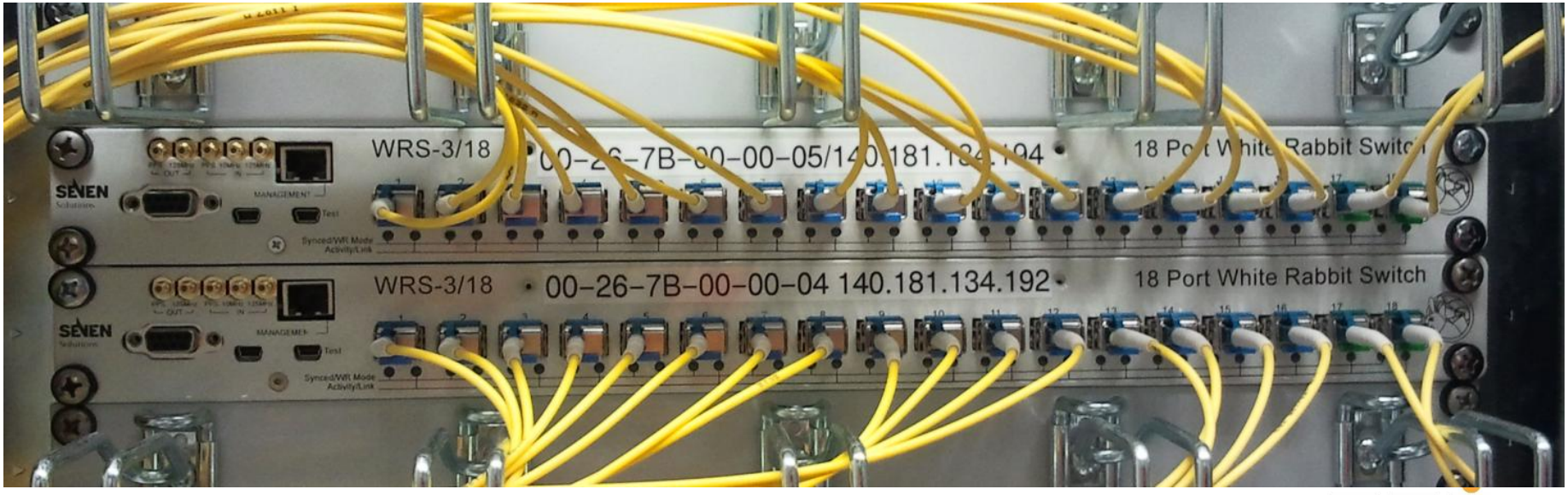
- carrier board with Arria GX II, **WR**,...
- COM Express™ module as mezzanine
- add-on board for interfaces
- “SCU-Bus” master in custom 3U crates
- > 1200 units at FAIR, equipment control
- developed in-house
- experience:
  - VHDL and C codes of White Rabbit PTP are portable!
  - non-open hardware can be linked to open hardware
- SCU is **the** reference for all timing receivers at GSI and FAIR!

Requirements for other form factors supported by CSCO

- form factor independent part: identical schematics & components
- form factor dependent part: identical concept
- otherwise: maintenance of firmware not manageable

Timing Network

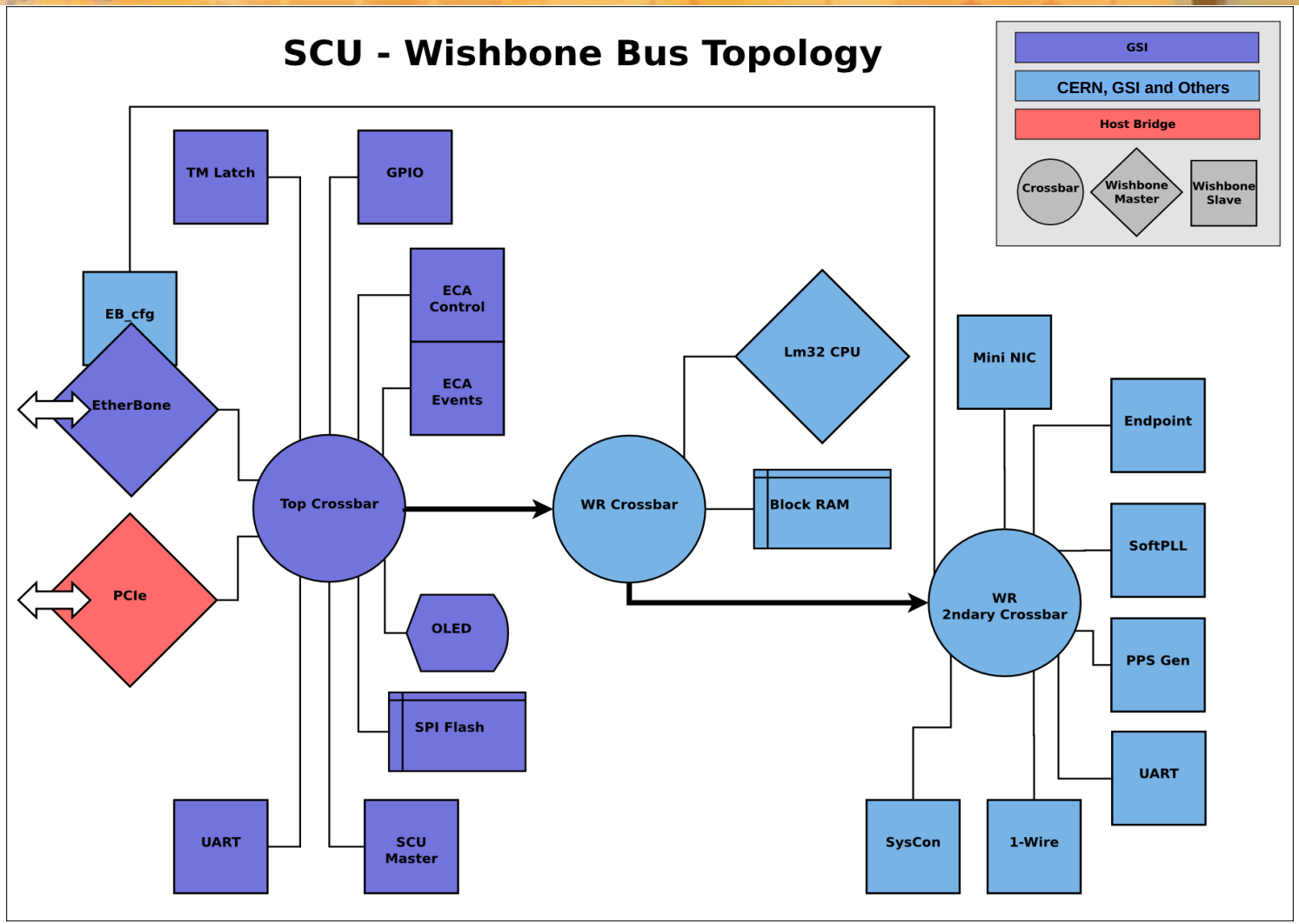
- based on standard V3 White Rabbit switches
- switches are very important!
- available under the terms of the CERN Open Hardware License
- produced and supported by industry
- experience: took a bit longer than expected – now a product
- “open”: functionality can be adapted to our needs!



Experience with Open Hardware
Here: White Rabbit PTP @ ohwr.org

- we joined the project in the design & development phase
- commercial hardware
  - let companies do what they can do better (CE certification, ...)
  - buy a products ready to use, including support (WR switches, ...)
- open hardware – it is in our own hands
  - ability to contribute to the requirements
  - not bound to specific manufacturer
  - can be integrated/interfaced into custom developments easily
  - long term: we could maintain, change, support for many years
- reconfigurable hardware
  - functionality defined by gateware (VDHL) & firmware (C)
  - need combination of open hardware and VDHL/C
  - development effort of VHDL/C and hardware is about the same

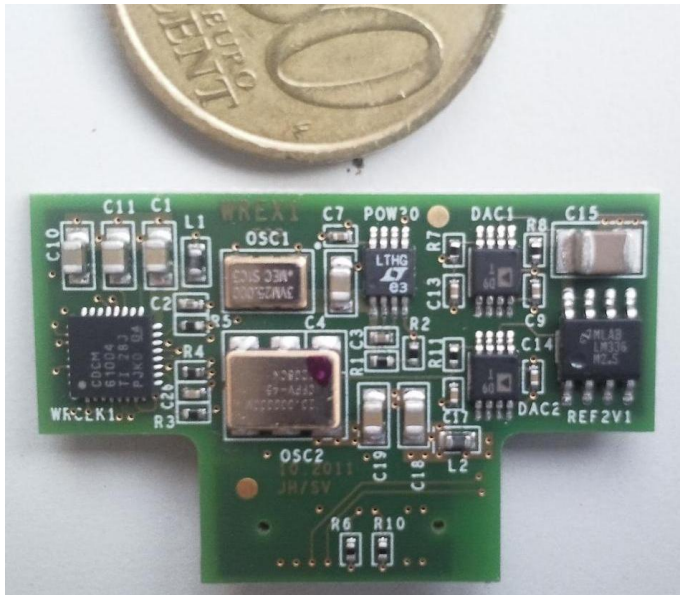
GSI's Contribution to ohwr.org
Here: Inside the FPGA



Example: EtherBone – extends on-chip Wishbone bus to outside world

Short Term Strategy for Timing Nodes of Form Factor other than SCU

- we (CSCOTG) are no HW developers
- “recycle” existing configurable hardware
- here: DAQ boards by CSEE/GSI based on Altera Arria FPGAs
- WR enabled by WREX1 add-on board



- experience: information from ohwr.org available and complete – success in the first try

- intermediate solution until final nodes are available
- further use by DAQ systems (?)

Perspectives: Open Hardware Contribution

Other form factors

- µTCA, PMC, 2x standalone, PCIe, VME
- 500 units to be delivered for FAIR
- main user: beam instrumentation group (LOBI/GSI)
- developed and built as in-kind contribution (Slovenia)
- “SCU compatibility” for ease of gateware/firmware maintenance (Altera FPGA ...)
- expected to be available under the terms of the CERN Open Hardware License

Summary

- user of open hardware
- contribution to WR development by gateware, software and money
- hardware contribution within the FAIR project is expected
- experience is very positive
- nice to have: more and larger companies offering WR products
- important: on-going standardization efforts

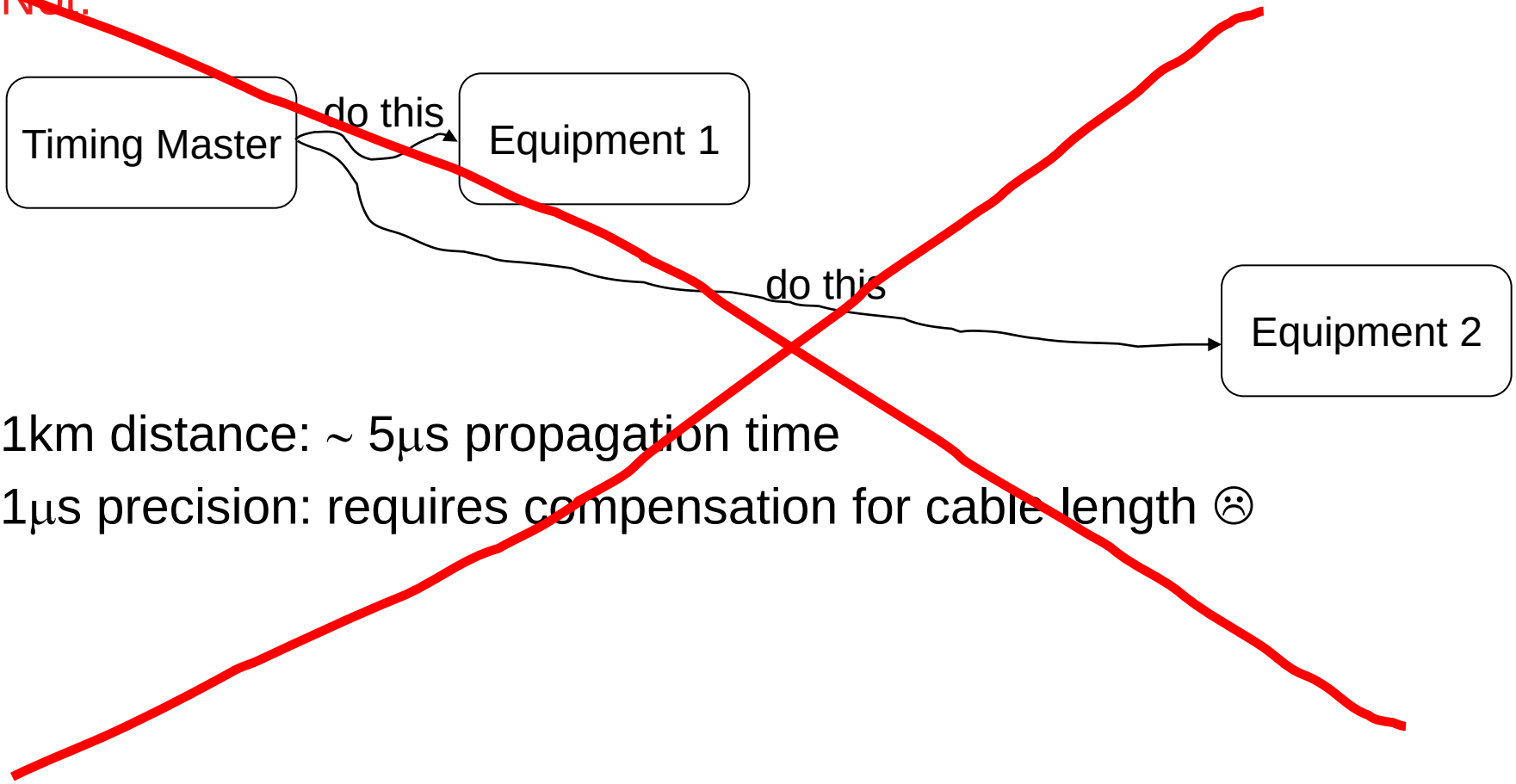
Thank you for your attention...

Status -“Proof of Principle”

- Clock Master: using GPSDO and/or BuTiS as reference clocks
- Data Master (message generation):
  - one machine only, no interlocks et al.
  - using Scalable Control Unit (FAIR standard controller)
  - implemented in lm32 in FPGA (no OS, hard real-time)
- Network:
  - 18 port White Rabbit switches (production quality, from “7 Solutions”)
  - no Forward Error Correction, no redundancy, ...
- Nodes based on Altera FPGAs (signal/IRQ generation):
  - SCU: in-house development by CSCO, o.k.
  - EXPLODER2C: standalone, in-house development by CSEE, o.k.
  - VETAR1: VME, in-house development by CSEE, needs revision
- VHDL and Software
  - some key components exist, ...

Idea: Timing System Based on Time

Not:

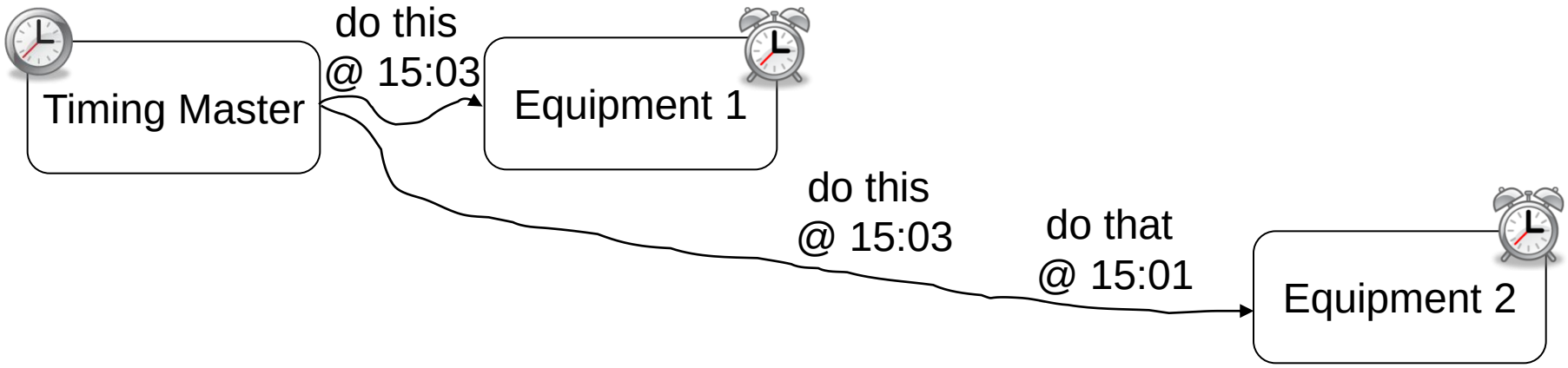


1km distance: ~ 5μs propagation time

1μs precision: requires compensation for cable length ☹

Idea: Timing System Based on Time

Instead:



- equipment pre-programmed for autonomous action at a given time
- action scheduled via timing-messages
- required: clock synchronization ~ns

⇒ distribution of information and execution of action are decoupled !!!

- timing-events must be sent “early enough”
  - upper bound latency for transmission (e.g. 100 μs): real-time!
  - lossless transmission: robustness!

White Rabbit "Fieldbus" Cooking Recipe

- network: Gigabit-Ethernet
- PTP (Precision Time Protocol) IEEE1588-2008
  - free-running oscillators on network nodes
  - need to re-sync often: lot's of traffic, bad for determinism
  - only 1-100 μs synchronization of clocks
- SyncE (Synchronous Ethernet)
  - receiver's clock recovered from 125MHz carrier
  - 8ns precision
- precise phase measurement and adjustment
- (dedicated switches for clock propagation across a network)
- clock synchronization with sub-ns precision and low-ps jitter using optical fiber (no copper!)
- Philosophy: Open Hardware and Software (www.ohwr.org)