

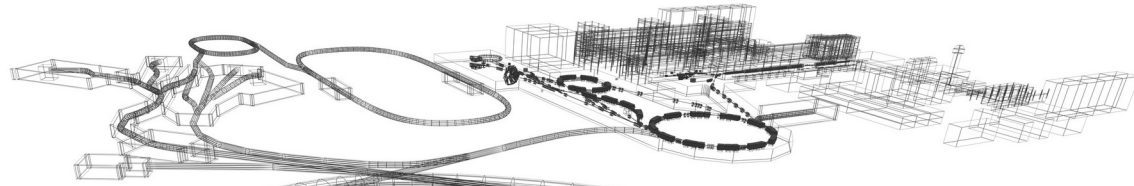
Acknowledgements



- GSI Timing Team: Enkhbold Ochirsuren, Marcus Zweig [1], Stefan Rauch, Mathias Kreider, Martin Skorsky, Dietrich Beck, Frederic Ameil [2], Anna Ranz, Alexander Hahn, Michael Reese
- GSI ACC-IT Team: Maxim Itterman, Peter Pfister, Christoph Handel, Rosemarie Vincelli ...
- CERN Team: Greg Daniluk, Maciej Lipinski ...
- External: Alessandro Rubini, Adam Wujek ...
- ...

[1] Michael, Martin and Marcus left; job opportunity https://www.gsi.de/en/jobscareer/job_offers

[2] Frederic is our new team leader :-)



WRC Related Activities at GSI

- Short Overview
- Timing Receiver Node Form Factors
- New Form Factors
- What About WRPC v5?
- WR Switch firmware

GSI from the Control System Perspective



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CRYRING

UNILAC

ESR

Fragment
Separator

SIS18

- 'FAIR Control System' including GMT (White Rabbit) @ GSI campus
- since 2016: CRYRING, (ring, ions-sources, Linac)
- since 2018: SIS18, ESR, all beamlines
- since 2022: synchronization of transfers between all ring machines
- fall 2024: machine experiment - beam production at UNILAC

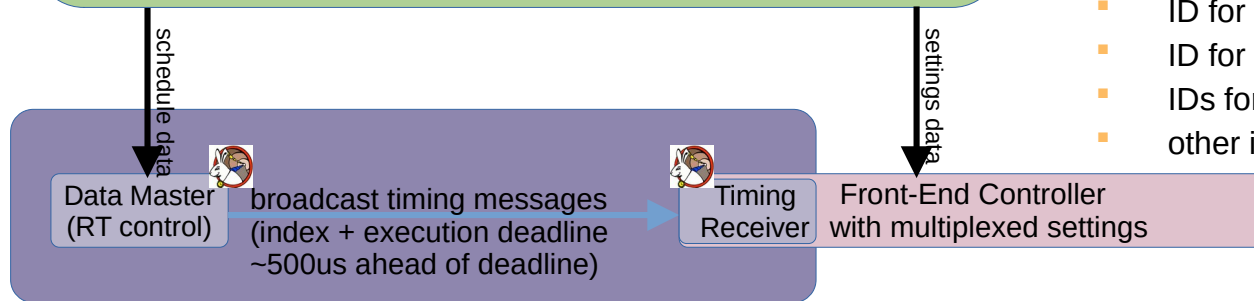
Multiplexed Operation, Control System Stack and General Machine Timing



Settings Management and Data Supply

Settings

- Front-Ends: set-values + indices
- GMT: real-time schedules + indices



Multiplexed Operation

- multitude of beams for many experiments simultaneously
- fast 'switching' between beam destinations and properties (element, neutron number, charge state, energy, intensity, focus ...)
- ring machines: 1Hz switching
- UNILAC: 50 Hz switching

Indexing Concept

- ID for area, location (,where')
- ID for action (,what to do')
- IDs for multiplexing context (,which beam')
- other information

General Machine Timing System:
trigger Front-Ends with multiplexing index on-time

Common Features for Timing Receiver Nodes 'Everything Happens in the FPGA'

no application specific VHDL!

instead:

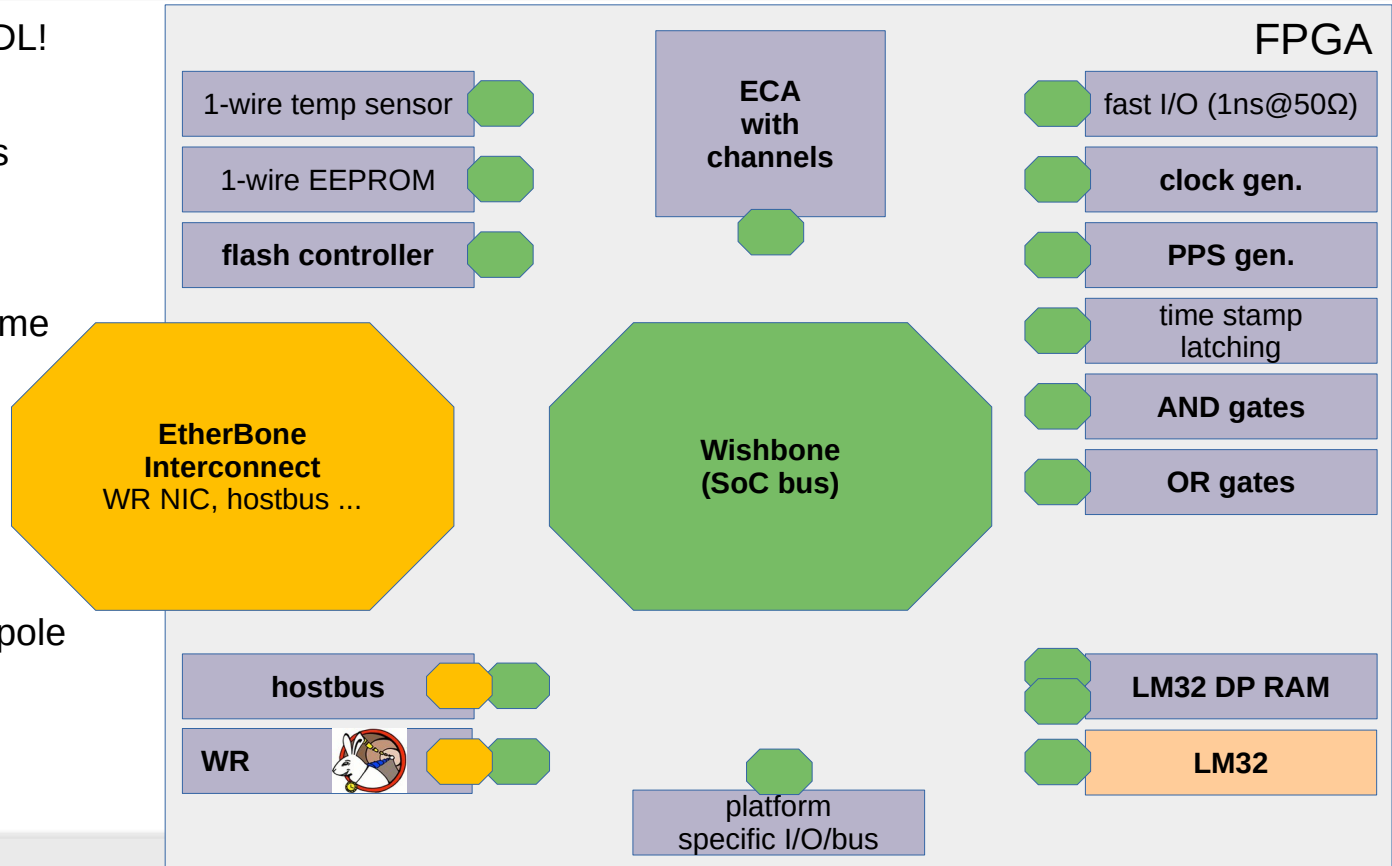
- configuration of IP cores
- ECA
- LM32 user softcore:

upload binaries at run-time
(c-code, OS-less)

hard real-time

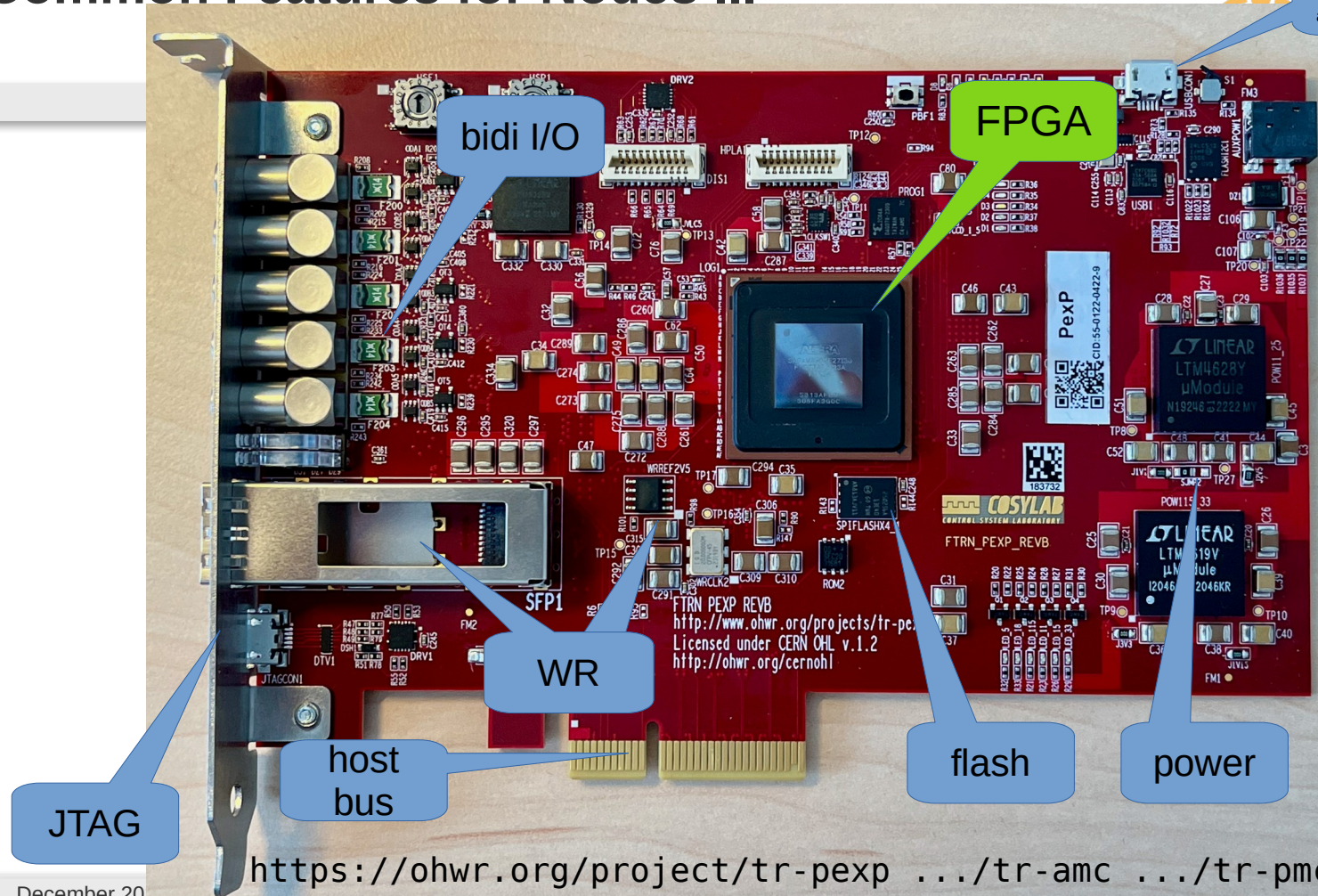
synchronosly at
many nodes

example: ramping up dipole
magnet current or
rf-cavity frequency



Common Features for Nodes ...

USB
another hostbus



<https://ohwr.org/project/tr-pepx> .../tr-amc .../tr-pmc

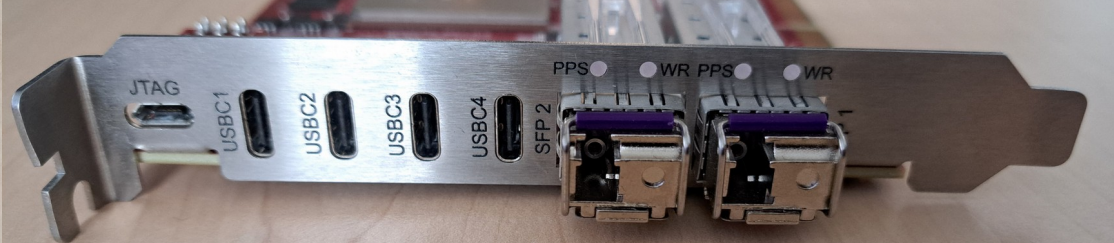
- 67 69 (104 107) [333] WR switches for facility operation (in use) [on-site]
 - mainly Creotech and Seven Solutions, some SyncTechnology
 - v6.1 for all operational WRS
 - SFP, mainly CBO with DDM
- 332 (416) [2296] WR nodes for facility operation (in use) [on-site]
 - OHWR: TR-PMC, TR-AMC, TR-PEXP; in-house: **SCU** (**S**calable **C**ontrol **U**nit, workhorse)
 - Arria V GX, Arria II GX
 - wrpc-v4.2
 - https://github.com/GSI-CS-CO/bel_projects, current release v6.3.1 ,fallout'
- host systems
 - SCU: COM Express
 - non-SCU: uTCA, VME, IPC (1U), Server-PC, other
 - PXE boot of ,ACO-Ramdisk' for **A**ccelerator **C**ontrol system
 - other

New Timing Receiver (TR) Nodes I



- Arria II – about 1/3 of TR at GSI, mainly SCU3; old FPGA type
- Arria V – about 2/3 of TR; formfactors 2x PCIe, AMC, PMC, standalone
 - availability on the market is bad (feels like it becomes deprecated)
 - maintaining gateway releases (FPGA images) requires a lot of effort
 - many units and functionality inside our images
 - use ‚seed mining‘ to make the fitter happy somehow
 - synthesis only possible with additional flip-flops and clock crossings
 - not yet: dedicated platform for Data Master
- A 10 – next generation Timing Receivers
 - SCU5
 - successor of SCU3, standard front-end controller for FAIR
 - in-house development
 - Pexarria10, two versions with different FPGA sizes
 - small: node version with one SFP/White Rabbit interface, 2 user soft cores
 - large: "Data Master" version with two SFPs/White Rabbit interfaces, 8+ user soft cores
 - same FPGA footprint for both
 - open source project on OHWR/GitHub/GitLab

- A10 TR to be contributed to WRC; relevant repos general-cores, wrpc-sw, wr-cores
- issues
 - when the large FPGA is used, heating is a major issue
 - dual White Rabbit kills PCIe, hard to fix, according to Intel/Altera problems inside the transceiver banks
 - 1ns LVDS IOs do not work yet
 - prime feature for TR nodes at GSI/FAIR (we don't use 'fine-delay' modules)
 - 1ns granularity achieved by using differential 1Gbit transceivers
 - time stamping
 - pulse generation
 - porting from Quartus 18 to Quartus 23 requires a new hardware revision (clocking)
 - only one 3V bank (not 3.3V!) -> level shifter madness



- works on Arria2 and Arria10
- ArriaV: WR unreliable – frequent loss of lock
- Etherbone partially broken
- to be contributed to WRC; relevant repos general-cores, wrpc-sw, wr-cores
- requires a major gateway release
 - for all (lots!) form factors used at GSI
 - not only WR, but other GSI/FAIR specific things too
- lower priority than development of A10 Timing Receivers
- not for 2025, 2026 maybe ...

- 21-22 Nov 2024: firmware update of all 107 White Rabbit switches from v6.1 to v7.0
- required changes in dot-config and new calibration parameters
- worked out very well
- only issue so far
 - „Error wrsSwcoreStatus: Endpoint TX frames number (462775) on port 10 (wri 10) does not match the number of frames forwarded from other ports (134005) and NIC (1090), some frames got lost... Difference is **more than 5**, since last check (293s)“
 - false positive
 - issue shows up only in a dedicated network with frame rates 1.5 ... 2.5 kHz
 - v6.1: less than 10 occurrences per **week**
 - v7.0: more than 100 occurrences per **hour**
 - proposal: configurable limit via dot-config (presently fixed limit of 5 frames)
- BTW: are there new calibration values for the fanless WRS from SynchTech?

logstash DQL Refresh

+ Add filter



Time	host	message
> Nov 27, 2024 @ 23:59:28.023	nwt0285m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (458646) on port 7 (wri 7) does not match the number of frames forwarded from other ports (326488) and NIC (1885), some frames got lost... Difference is more , since last check (291s)
> Nov 27, 2024 @ 23:59:28.022	nwt0285m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (458628) on port 3 (wri 3) does not match the number of frames forwarded from other ports (391997) and NIC (1095), some frames got lost... Difference is more , since last check (291s)
> Nov 27, 2024 @ 23:59:28.020	nwt0285m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (458598) on port 2 (wri 2) does not match the number of frames forwarded from other ports (391997) and NIC (1065), some frames got lost... Difference is more , since last check (291s)
> Nov 27, 2024 @ 23:58:56.653	nwt0291m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (468202) on port 14 (wri 14) does not match the number of frames forwarded from other ports (278519) and NIC (1075), some frames got lost... Difference is more 5, since last check (296s)
> Nov 27, 2024 @ 23:57:55.486	nwt0292m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (468481) on port 6 (wri 6) does not match the number of frames forwarded from other ports (393861) and NIC (1084), some frames got lost... Difference is more , since last check (292s)
> Nov 27, 2024 @ 23:57:10.249	nwt0100m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (462440) on port 10 (wri 10) does not match the number of frames forwarded from other ports (395829) and NIC (1075), some frames got lost... Difference is more 5, since last check (293s)
> Nov 27, 2024 @ 23:57:10.248	nwt0100m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (462452) on port 9 (wri 9) does not match the number of frames forwarded from other ports (395829) and NIC (1087), some frames got lost... Difference is more , since last check (293s)
> Nov 27, 2024 @ 23:54:29.781	nwt0285m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (393225) on port 6 (wri 6) does not match the number of frames forwarded from other ports (457677) and NIC (1084), some frames got lost... Difference is more , since last check (290s)
> Nov 27, 2024 @ 23:54:00.340	nwt0291m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (468289) on port 14 (wri 14) does not match the number of frames forwarded from other ports (336132) and NIC (1085), some frames got lost... Difference is more 5, since last check (297s)
> Nov 27, 2024 @ 23:52:17.582	nwt0100m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (462834) on port 10 (wri 10) does not match the number of frames forwarded from other ports (199618) and NIC (1072), some frames got lost... Difference is more 5, since last check (293s)
> Nov 27, 2024 @ 23:52:17.581	nwt0100m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (462836) on port 9 (wri 9) does not match the number of frames forwarded from other ports (265154) and NIC (1074), some frames got lost... Difference is more , since last check (293s)
> Nov 27, 2024 @ 23:52:03.643	nwt0292m6	SNMP: Error wrsSwcoreStatus : Endpoint TX frames number (455127) on port 6 (wri 6) does not match the number of frames forwarded from other ports (388524) and NIC (1067), some frames got lost... Difference is more , since last check (288s)

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- GSI joined WRC in November 2024
- working on new hardware platforms based on Arria 10 FPGAs
- working on migration to WRPC v5 (low priority)
- updated all WRS to v7.0

Thank You For Your Attention