

# **FAIR**

## **Accelerator Control System**

### **Baseline Technical Report**

Prepared by the GSI Controls Group (BEL) Design Team

Author: T. Fleck

Editor: R. Bär

#### **General Machine Timing (GMT) System**

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# FAIR Accelerator Control System Baseline Report

## Document Structure

The FAIR Accelerator Control System Baseline Report gives a detailed technical and engineering overview of the accelerator control system (ACS) for the FAIR/GSI facilities. The Baseline report comprises executive overview documents as well as a series of documents which provide detailed descriptions and performance of technical aspects or subsystems of the ACS. In addition to that there are a series of supplemental documents and appendices.

The Control System Baseline Report consists of the following comprehensive documents.

### Overview Documents

- General System Overview
- Technical System Overview

### Technical Parts

- Equipment Interfaces and Device Control
  - Front-End Software Architecture
  - **Timing System**
  - General Application Framework
  - Accelerator and Beam Setting Generation and Management
  - Communication Middleware
  - Industrial Controls
  - Control Center and IT Infrastructure
  - Interlocks and Machine Protection
  - Control System Services
  - Data Management and Database Services
- 
- Integration of the Present GSI Control System

### Appendices

- Control Architecture Glossary

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# 1 Content of this Document

In its current version this document describes the general layout of the timing and event distribution system for all FAIR accelerators and beam lines with the main focus on the distribution system itself. In the next version of this document more details about the timing master, event generation and Interfaces shall be given.

In Chapter 2 ("Timing System Overview") general requirements to the timing system are listed and the chosen technology is described together with a description of collaborations in this area.

Chapter 3 ("Specification, Features and Constraints") describes global use cases of the timing system, how event distribution is implemented and states limits of the timing system to be checked against all the requirements from different groups.

In Chapter 4 ("Implementation Design") details about the architecture are given and the main components of the timing system are described.

Chapter 5 ("Interfaces") finally describes all interfaces to the timing system and Chapter 6 lists requirements from the timing system to a central control system database to store and/or interchange information. Chapter 7 finally lists some of the open questions / topics.

## 2 Timing System Overview

### 2.1 General Requirements

Within each accelerator of the FAIR complex all beam guiding components have to be triggered synchronously with an accuracy of at least  $1\ \mu\text{s}$ . The same holds for all beam diagnostic devices while the requirements to rf components regarding synchronization and simultaneity are three to four orders of magnitude higher.

All components set values or ramp data for several virtual accelerators are preloaded in the front-end controllers<sup>1</sup>. The timing system ("general machine timing" / GMT) has to trigger and synchronize all equipment action in real-time and provide all necessary information like virtual accelerator number, machine ID and event number.

Moreover the different accelerators and beam transfer sections in the FAIR facility have to be tightly synchronized for all beam transfers. Several types of beams with a variety of properties (ion type, energy, intensity) will be present in the FAIR machines at the same time, thus the FAIR facility implies a high degree of true parallel operation. Individual cycle lengths range from 20ms (present UNILAC) to several hours (storage rings) with cycle lengths of several seconds in the accelerators.

Since the current GSI accelerator chain can be reckoned as a kind of injector for FAIR and since the GSI timing system will persist, the new GSI/FAIR timing system must additionally provide proper interfaces to orchestrate the current timing system and synchronize injection from SIS18 into the FAIR complex.

Altogether the timing system connects about 2000 timing receivers distributed about the whole complex, thus the signal path between the timing master and an individual timing receiver can be up to a few kilometers which cannot be neglected; instead signal propagation time has to be corrected or compensated.

The timing system must not only provide event resolution of at least  $1\ \mu\text{s}$  but must also be capable of follow-up events below  $10\ \mu\text{s}$ . An additional important requirement is absolute time stamping

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<sup>1</sup> provided by the control system via a dedicated network

needed in most timing receivers for e.g. read value or interlock logging. The absolute date and time provided by the GMT will be correlated to UTC.

For high precision synchronization as needed for the rf-components, a separate system called BuTiS (Bunchphase Timing System), will be installed. Therefore the absolute timing requirements for the GMT are relaxed, but the BuTiS system has to be properly integrated in the GMT.

Each FAIR machine will need a (at least logically) separate timing event generator to generate all timing signals for a dedicated accelerator cycle within this machine. Information about the beam to be handled next has to be broadcasted as well and alternate event tables have to be supported.

Additional real-time information like read values of beam current can also be handled (received and sent) within the timing system and the possibility of soft-Interlock-handling is foreseen. Also an indirect exchange of short telegrams between selected timing receivers will in principle be possible since this might be needed for e.g. bunch to bucket transfer.

A master cycle sequencer is necessary to coordinate and orchestrate all beams and cycles throughout all GSI / FAIR accelerators. It has to synchronize all machine timing event generators and establish patterns of beams. General restrictions, emergency or non-availability situations have to be handled by it making use of alternative beam delivery scenarios.

Timing event receiver functionality has to range from simple units that will e.g. output manually selectable events as TTL pulses to highly integrated devices like the front-end controller to be used within the power supplies. Also different form factors will be provided.

## 2.2 Choice of Technology

The timing distribution system will be a dedicated network based on the following key technologies and protocols (but will not be compliant with all details of these standards):

- Synchronous Ethernet (clock distribution, frequency synchronization)
- Precision Time Protocol PTP; IEEE standard 1588 (time/date, coarse time synchronization)
- Gigabit Ethernet GbE (transmission standard over fibre and copper)
- SNMP (Network management)
- White Rabbit Control Message Protocol WRCMP

Connections will be realised using standard fibre and copper transmission lines. All connections within the timing system use fibre optics with an additional redundant connection while all connections to timing receivers are single-line using either copper or fibre.

Special layer 2 switches, so-called "white rabbit" (WR) switches, will be designed and used following the new layer-2 "white rabbit" protocol standard described in detail in the following chapters. The complete timing network will be carried out in tree topology with most probably three layers of switches.

All timing receivers must be WR compliant devices in order to be able to receive and decode distributed timing telegrams. The timing network will only have few and well-specified interfaces to non-WR compliant devices like hardware interlock signal inputs or communication between the control system and the timing master.

The timing system will distribute an absolute time correlated (but not identical) to UTC via the usage of an external GPS and/or Galileo receiver and synchronize each single timing receiver with this absolute time with an accuracy exceeding the requirements of all systems besides the rf system. To comply with rf requirements the timing system will furthermore be synchronized with an rf BuTiS clock. There will be no real transmission delay compensation but instead signal propagation is accounted for in the process of synchronizing all timing receivers to this absolute time. In addition the timing system will not be an true event based system, i.e. event execution will not start immediately upon event receipt. Instead execution times will be transmitted.

With the synchronized local clock data can be time-stamped well beyond the microsecond level.

The system timing master will broadcast all centrally generated timing telegrams campus-wide to all timing event receivers. Thus even events that are only valid for one machine can be decoded and used by any timing receiver campus-wide.

For the transmission of timing telegrams forward error encoding (FEC<sup>2</sup>) will be used since the requirements to timing do not allow for any kind of handshake.

The timing system will use the concept of so-called granularity windows that will be transparent to timing system users: The timing system will broadcast one event stream at the start of each granularity window containing all necessary events for the next window.

## 2.3 Collaborations / Shared Developments

WR protocol and WR switch specification are a result of a collaboration between different institutes and companies, mainly CERN and GSI, to fulfil all necessary requirements for control system usage - especially determinism and time accuracy.

The so-called "Timing Hardware Project" was initiated by people from CERN in March 2008. Its main goal is to find and develop a common solution for a timing distribution system to the maximum extent in close collaboration of several institutes<sup>3</sup>.

The evolving standard of the project is called "**white rabbit**" and comprises

- A layer 2 protocol being capable to fulfil all requirements from different institutes regarding especially latency, determinism, synchronicity and scalability.
- Specifications for all necessary hardware: switches, front-end controllers, timing master including PCB layout, VHDL code, coding styles etc. in the framework of an open hardware repository.

All hardware prototypes have to be developed by project members where CERN focuses on the WR timing switches and GSI on the WR timing master.

### Official Project description

[...White Rabbit (WR) is a solution to the generic problem of transferring data in a fast, deterministic and safe manner. Although its initial scope is mainly targeted at timing systems for experimental physics facilities, care has been taken in the protocol specification to come up with a solution which is as generic as possible...]

### Collaborations

- partners: CERN, GSI, AAS, IN2P3, ELETTRA, Cosylab
- possible participators: NUSTAR experiments, ITER, medAustron and whoever else interested in joining

### Shared development and specification include

- OHR (open hardware repository)
- VHDL, PCB design, SW, specifications, coding styles
- usage of the same hardware at participating institutes:
  - timing receivers
  - WR switches
  - timing master

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<sup>2</sup> Within this document FECo will be used since FEC is also used as shortcut for Front-End Controller

<sup>3</sup> In spring 2008 the company Cosylab carried out a study where requirements from different institutes have been compared.

## 3 Specification, Features and Constraints

### 3.1 What is the GMT used for (Use Cases)?

- The GMT will broadcast all necessary timing events with additional meta information to all timing receivers taking into account different signal propagation times. Timing telegrams contain e.g. virtual accelerator numbers and thus indicate directly which data set has to be used by individual front-end controllers.
- The GMT can be used to transmit online cycle status like beam current from a timing receiver to the timing master, the control system or all timing receivers. In such a case "high priority" packets (see following section) will be generated by a timing receiver, sent up to the timing master<sup>4</sup> and will be included into the next timing telegram. Thus the information is known by each timing receiver and in addition the sender uses this as acknowledge. In addition the timing master can route this information to further systems like the control system.
- The timing system will allow for frequent changes in beam pattern, several parallel experiments and different interleaved beams. Pulse to pulse beam switching will be supported using corresponding events.
- Distinct beam identifiers (e.g. virtual accelerator numbers) will be used.
- Since events are sent shortly before the reaction time they are always sent in running cycles. This eases modification of cycle sequences. Also choice of next cycles will not only base on predefined beam patterns but will also include current machine status information.
- The GMT provides synchronous clocks for all timing receivers in phase with BuTiS  $T_0$  clock.
- All WR timing receivers decode the same timing telegrams and can react on any information within according to their individual programming and set-up.
- The GMT synchronization all connected devices (switches and timing receivers) to an absolute time defined by the timing master that is used as facility-wide standard. With this feature all timing receivers can timestamp all relevant data with an accuracy well beyond the specific needs: Time synchronization is in the sub-ns range; at least three orders of magnitude better than requirements to timestamping.
- ...

### 3.2 What the GMT cannot be used for / cannot provide

- The GMT will not provide PoE (Power over Ethernet), thus every timing receiver must host its own power supply.
- The timing system is constructed as a dedicated physical network and must not be used by other devices than WR timing receivers or special WR diagnostic devices. More details in the following chapter 3.5.
- Event receipt and decoding will not take place synchronously in the timing receivers; synchronicity is achieved only via distribution of trigger action times in combination with clock synchronization.
- Although timing receivers (TRs) can use the timing systems upload possibility to share important information with the timing system, other TRs and the control system, this will be only possible for few special devices and well defined important information with high real-time and reliability requirements.
- Contrary to the BuTiS system the TRs of the GMT will not feature oscillators with highest stability. In the case of lost connection to the GMT the accuracy of a timing receivers timestamps will gradually decrease with time. Requirements to e.g. post-mortem analysis of

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<sup>4</sup> Reminder: Open WR protocol detail issue: HP generally broadcasted

an individual TR therefore have to be taken into account when defining individual TRs oscillator quality.

- ...

### 3.3 Event Distribution

The timing system will know two types of messages to be sent and received:

- Normal Ethernet frames called SP packets (standard priority). To this class belong all non timing critical messages like PTP clock synchronization, SNMP or further WR messages.
- "high priority" HP packets, mainly timing telegrams. HP packets will be broadcasted deterministically with well-defined switch latency time.

To be able to assure determinism of HP packets, all other SP-traffic will be fragmented, i.e. paused upon arrival of any HP packet; this is one of the main WR specific feature.

The timing master broadcasts "event streams" every 100 $\mu$ s at the beginning of each granularity window where its size will eventually be only 50 $\mu$ s, but at any rate a multiple of 10 $\mu$ s because of necessary BuTiS synchronization.

Each event stream consists of an header and several events. With each event the information at which exact time it has to be executed is transmitted. Each event will be sent in the granularity window preceding the event time, although this is no general constraint.

An event will consist of 12Byte including 4Byte event IDs and 8 Byte event payload. Although the event content is not yet defined this size is accepted to fit all upcoming requirements to the timing events. Each event stream has a minimal length of 200Byte (due to requirements from FECo algorithm and reliability considerations) but can be larger, thus at least 10 different events can be transmitted within one granularity window taking into account an additional event stream header containing meta-data like e.g. UTC second and status information. Neither the event stream headers content nor status information to be broadcasted have yet been discussed or defined.

Even if no events for the next granularity window have to be send an "empty" event stream will be sent to be used e.g. as heartbeat for all timing receivers.

Since no loss of events is acceptable<sup>5</sup>, some special implementation of forward error correction (FECo) is used: Following standard FEC methods some algorithm like LT coding is implemented in a way that each timing telegram is divided into a couple of sub blocks where some of these sub blocks are XORed. Using additional redundancy several follow-up Ethernet frames thus are broadcasted. They built up one timing telegram to be decoded by each single timing receiver. Dependent on the redundancy factor the receipt of only about half of all packets is sufficient to decode the original message. Owing to the FECo algorithm itself this is independent on which individual packets have been received. This is the key element regarding overall system reliability and stability.

In Figure 1 the concept of granularity windows and the distribution of timing telegrams is visualized. Indeed it's not improbable that around 20% of the total GbE bandwidth will be used by the timing telegram frames, but of course this is highly dependent on granularity window size, number of events to transmit per window or redundancy factor used.

It is noteworthy that the timing system is not an event-based system in the sense that event reaction will take place as soon as the events are received. Also the propagation delay compensation is performed indirectly through the usage of the granularity windows:

Event reaction is based on the synchronized local clocks while timing telegrams will reach different receivers at different absolute times well inside the same granularity window. The latter has to be

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<sup>5</sup> Maximum amount of lost or erroneous timing telegrams is in the order of one per year. This corresponds to 10<sup>-12</sup> of all telegrams and 10<sup>-15</sup> regarding the multitude of timing transmission lines.



guaranteed by the GMT through proper choice of all relevant parameters taking into account environmental boundary conditions (maximum fibre length, number of switch layers).

timing event messages  
 granularity windows concept

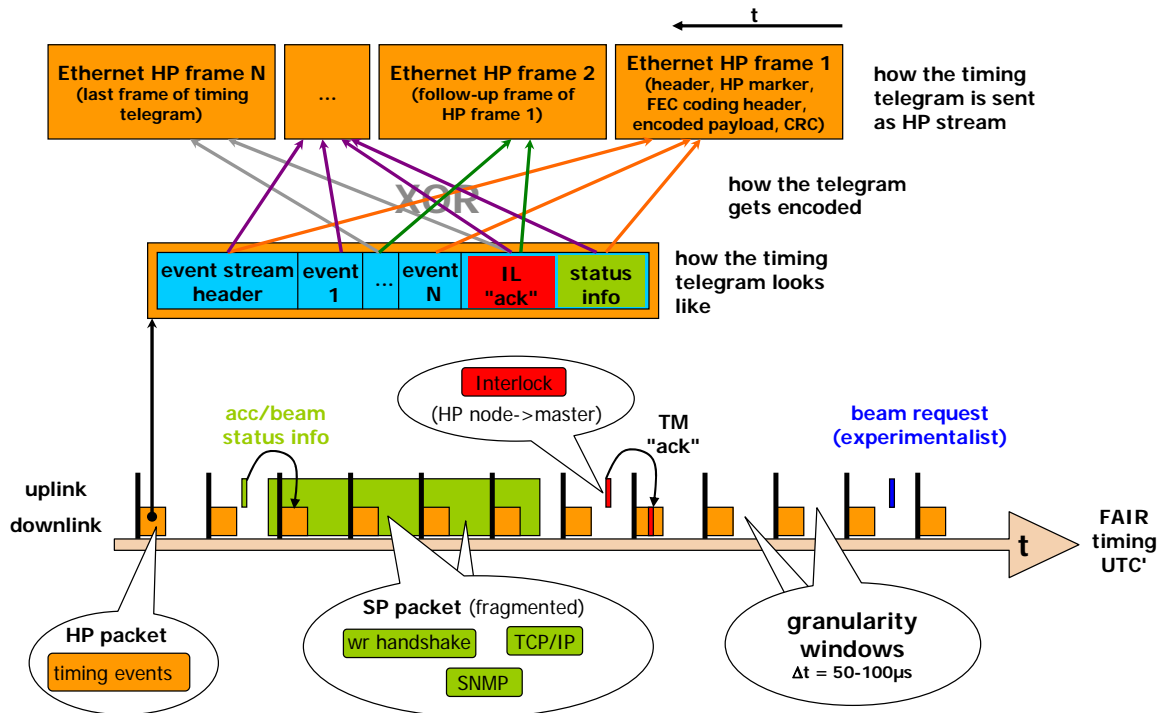


Figure 1: Granularity window concept and distribution of timing telegrams. Included is the possible usage of soft Interlock handling.

### 3.4 Overall Performance of the GMT

The signal propagation time from the timing master to the most distant node will be in the order of, but less than  $20\mu s$ : Signal propagation time is about  $15\mu s$  for 2km fibre length and about 500ns for 100m copper cable while the WR switch latency time equals 64Byte (512ns on GbE) for HP packets and a maximum of three layers of switches will be used.

The combination of granularity window size and signal propagation time gives the limit for the systems reaction time: In normal mode each telegram will be sent at the beginning of a granularity window and the defined reaction time span is the next granularity window.

If necessary it would be possible to send an "emergency event" at any time with the information that front end controllers have to react immediately. In this case only the sum of signal propagation times, latencies and times for encoding/decoding has to be taken into account. However, until now there is no known use case requiring faster reaction time than that defined above.

Upward HP information (like interlock or beam status) will reach all other timing receivers well within two granularity windows. If such a packet is received and decoded by the timing master shortly before the end of a granularity window, this time will of course be shorter, since the information will be sent within the next timing telegram.

#### 3.4.1 Additional Performance considerations

- The decoding of timing telegrams from the individual HP packets in combination with the analysis of individual TR event filters will take some time. It is assumed that this time is

negligible, especially since there are up to some ten micro-seconds time between receipt of the last HP packet of a timing telegram and the start of the next granularity window.

- In the case of a lost connection to any timing receiver it will take at least the time necessary for transmission from the last switch to the timing master before any reaction can take place. This time will be in the order of 15  $\mu$ s.
- 
- [...]

### 3.5 GMT Connections to Non-WR Compliant Devices

At the GSI/FAIR facility it is neither intended nor allowed to connect any non-WR compliant device to the timing network except of maybe a handful of well-defined and accepted devices. However, the WR protocol specification notes that a WR network should be fully transparent to “normal” Ethernet network traffic. But this functionality is more than questionable and rather unlikely and error-prone. It will simply be impossible to provide complete standard routing functionality in the switches. This topic will be discussed with the collaboration partners since not all use-cases of the collaboration partners are fully known.

The same question arises regarding e.g. the implementation of the special WR PTP (precision time protocol) implementation using special adapted “WRPTP” messages. However, fully compliance to PTP IEEE protocol standard seems achievable but use cases only exist in the case non-WR compliant devices connected to the WR network.

Anyhow the timing network will provide means not to stop working properly if any non-WR compliant device is connected to it. This is necessary, since normal Ethernet connectors (RJ45 and standard fiber connectors) will be used.

## 4 Implementation Design

### 4.1 Timing Network Architecture

The FAIR timing network will be carried out in a tree topology and connects one global system timing master to about 2000 timing event receivers. Some layers of timing switches – most probably three - using the WR protocol standard will be used, i.e. all switches will be true WR compliant devices. Form factor of WR switches is  $\mu$ TCA.

One redundant uplink channel for each switch is present (connected to the  $\mu$ TCAs MCH) that will be connected to the same uplink switch. The number of possible downlink connections to switches in the next layer is only half of the switches downlink ports if this redundancy is used. Each WR switch will have up to eight AMC modules with up to eight downlink ports each.

The layout of the system is shown in Fig. 2. Included in the figure are all timing receiver form factors supported by WR as well as functional blocks inside the timing master and general timing master inputs.

Connections will be realised using standard fibre and copper transmission lines. All connections within the timing system use fibre optics with an additional redundant connection while all connections to timing receivers are single-line using either copper or fibre. Connections have to comply to the according standard IEEE802.3z for GbE over fibre/copper. For copper connections 1000BASE-T as defined in IEEE802.3ab is valid requiring at least Cat5 cabling while 1000BASE-LX is valid for single-mode fibre connections.

## FAIR Timing System Architecture

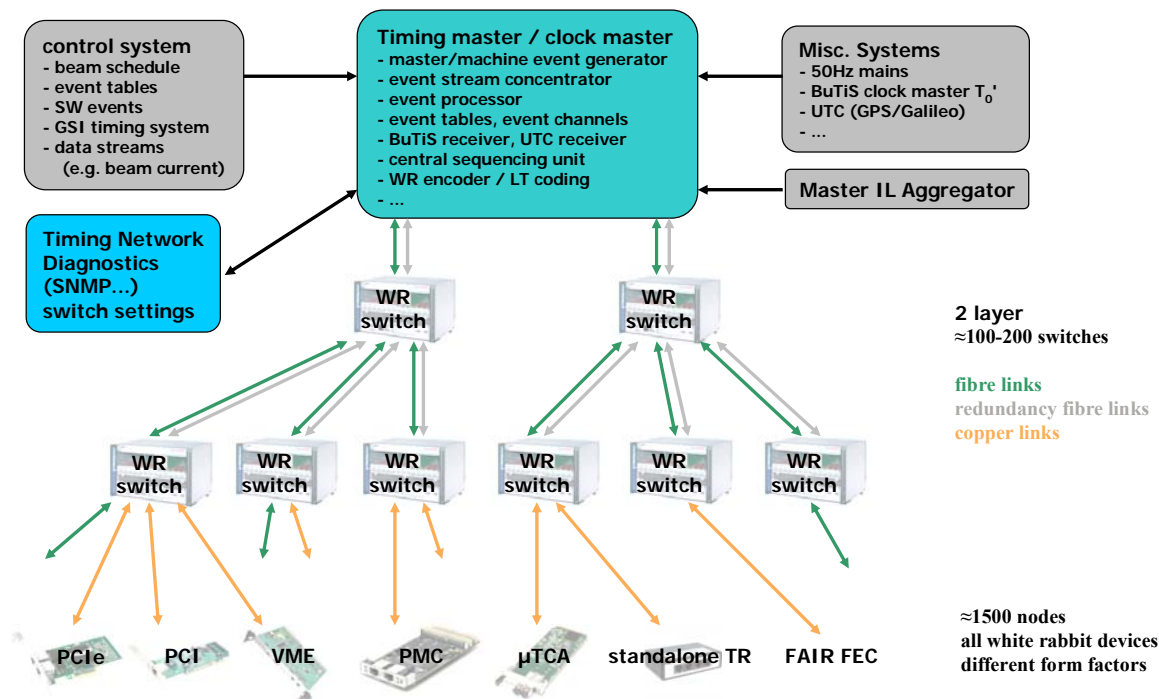


Figure 2: Architecture of the FAIR timing system showing all possible timing receiver form factors and principle timing master functionality and interfaces.

## 4.2 Timing Master<sup>6</sup>

[...]

### 4.2.1 Functional Blocks

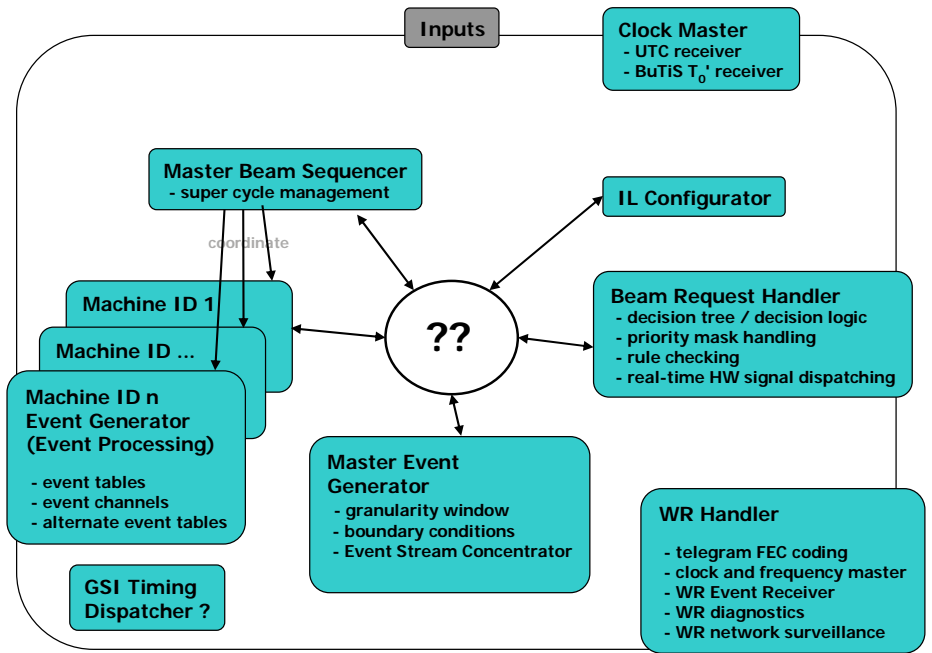
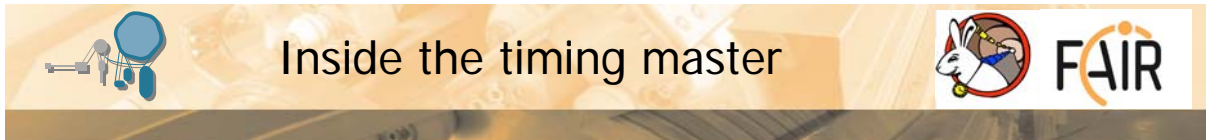
**Master Beam Sequencer** (synonyms: Central Sequencing Unit or Task scheduler): This is the central unit to coordinate and orchestrate all machine event generators (EVGs), thus all activities for the whole facility. It includes super cycle management, e.g. a beam defined in the super cycle that is not requested by the experimentalists or cannot reach its target properly must not be produced. It triggers the event generators to start execution of the appropriate cycles. Also non-predictive cycle extensions have to be handled. **The actual sequence of the accelerating cycles is not even known to the operator beforehand. [Has to be changed]**

- Determines, which beams have to be produced next. Conditions are e.g. requests or Interlock states.
- Channel synchronization
- **Machine Event Generator:** Event processing for a single machine or timing section
  - event tables (synonym: event channels): closed and have to be uninterruptedly played. Can be conditionally triggered. There may be up to 64 event tables per virtual

<sup>6</sup> This chapter contains currently no real design decision nor specification, rather it comprises requirements from several documents and first implementation thoughts including necessary WR timing master functionality and transferability to other facilities.

accelerator and per machine (?). In a VAcc concept with 16 VAccs per machine (not clear yet) this would correspond to  $2^{10}$  event tables. There will be a maximum time for each event table and a maximum number of events per table.

- Event tables will be started by external signals or the current super cycle initiated then by the MBS.
- alternate event tables; on the fly modification by external conditions --> parallel tables.
- An event table is a list of entries where each entry contains (i) name of the event, (ii) time to sent the event, (iii) execution time of the event, (iv) event payload.
- **Master Event Generator**
  - granularity window
  - event stream concentrator
  - boundary conditions (facility power load, mains synch.)
- **GSI Timing Dispatcher (?)**
- **Clock Master:** Receives UTC from a GPS and/or Galileo receiver. Also receives the BuTiS  $T_0'$  and possibly also BuTiS  $T_0$  and  $\delta t$ . Produces the absolute time UTC' and the frequency reference for the complete timing system.
- **Beam Request Handler** and rule checker; Real-time HW-signal dispatching and decision logic / decision tree, priority masks handling
- **IL Configurator**
  - inputs: master aggregator, soft ILs
- **WR Handler**
  - WR functionality itself
  - FECo coding algorithm / telegram encoder
  - Event Receiver and accelerator data stream dispatcher
  - WR diagnostics
  - WR network surveillance



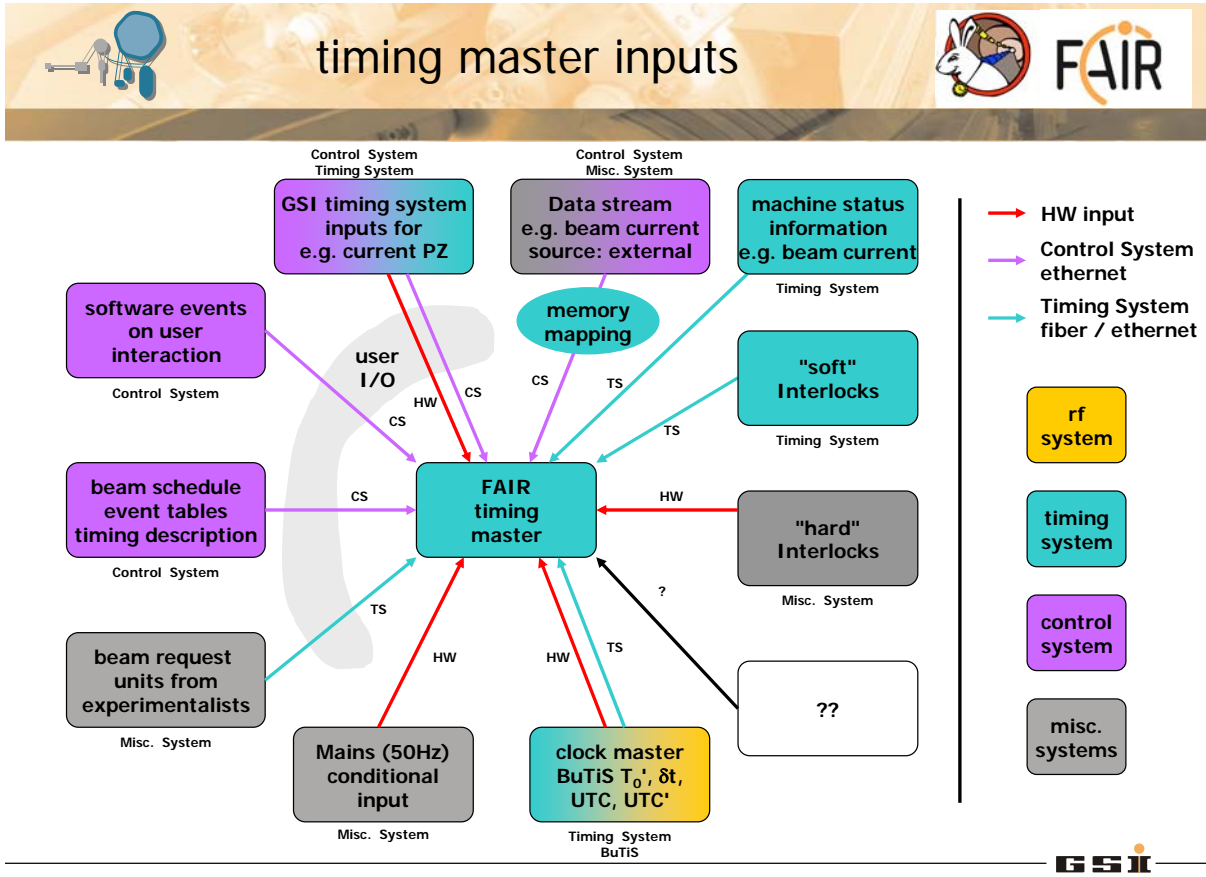
T.Fleck, GSI



Figure 3

### 4.2.2 Inputs

add database to figure  
 [...]



T.Fleck, GSI



Figure 4: Inputs to the timing master

### 4.2.3 Outputs

[...]

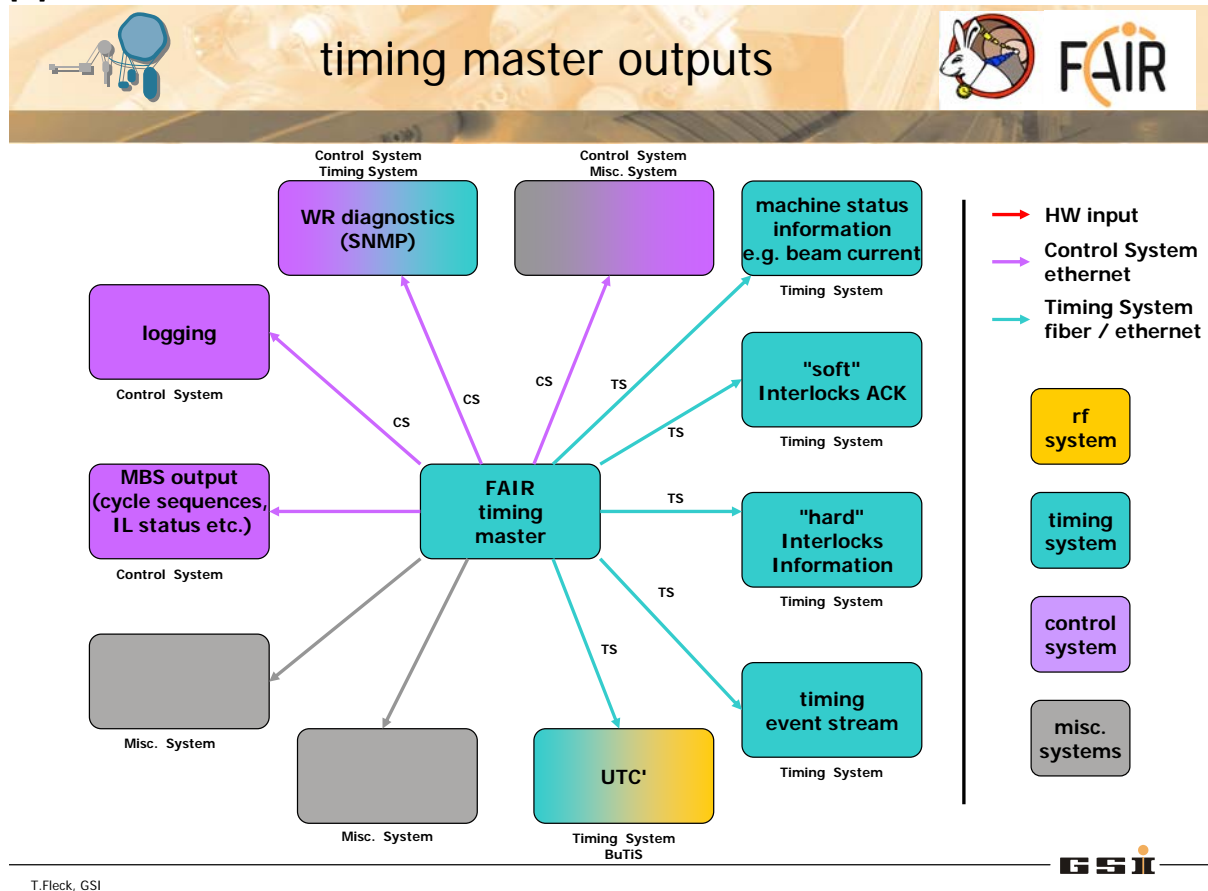


Figure 5

### 4.2.4 Outside Influences

50Hz mains; net phase synchronisation  
 maximum allowed facility power consumption  
 forbidden frequencies  
 [...]

### 4.2.5 Hardware, Hot Standby and Safeguarding

The decision about the hardware platform / form factor of the timing master is not yet taken. Decisions will be made at the earliest as soon as functional specifications are complete. Amongst others of course  $\mu$ TCA will be evaluated since this is the form factor of the WR switches and could be advantageous since the timing master has to be fully WR compliant and adaptation of common WR VHDL code could be easier.

Right now it is also totally unclear if the timing master will be a single device or several interconnected hardware devices, i.e. if a modular design with multiple masters will be used or not. This holds especially for the multitude of different event generators.

The timing master will be designed as a hot standby system. Three control cabinets are foreseen with two productive systems (switchable: active/standby) and one development system where one of the productive systems is the hot standby.

Each timing master will additionally provide:

- Front-Panel LEDs
- Diagnostic port
- Trigger outputs ?
- ...

[...]

### 4.3 Active Transmission Components

Active Transmission Components in the timing network are the WR switches in  $\mu$ TCA form factor.

[Details about implementation details, functionality, etc. following ...]

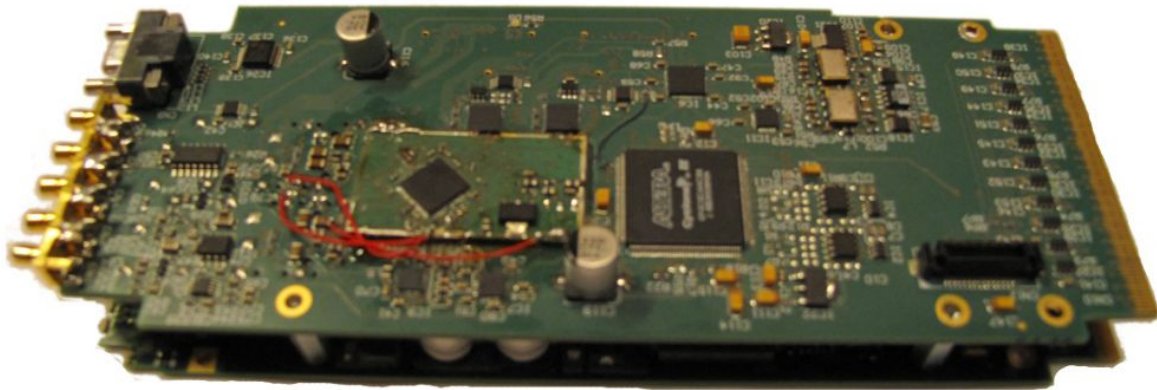


Figure 6: switch PCP board prototype (September 2009)

### 4.4 Timing Receivers

The range of WR compliant event receivers functionality spans from simple units that will output manually selectable events or event patterns as TTL pulses to highly integrated devices like the front-end controller to be used within the power supplies. They will be provided in different form factors and provide at least one copper or fibre GbE connector to connect to the timing network.

The following hardware platforms will be available for timing receivers:

- PCI
- PCIe
- VME
- PMC
- $\mu$ TCA
- simple standalone TRs

In general all timing receivers pick up every single HP packet and decode all original WR timing telegrams using "backward FECo" algorithm/logic.



They all synchronize to the absolute time provided from the timing master and provide relevant device status and message information via SNMP to the timing system. All Timing Receivers will have an individual IP address<sup>7</sup>.

Dependent on the individual timing receiver, following functions or combinations of them will be provided:

- Analysing the timing telegram
- Trigger front-end controller action for special selectable events
- Provide Hardware trigger signals filtered on e.g. event number, VAcc number, Beam number
- Provide complete undecoded event data stream
- Provide time of day and exact timestamps (UTC')
- Provide mechanisms for delayed reactions to some event. Responsibility is at the user side; correct parameterisation has to be ensured; most possibly special TRs will be provided as flexible delay units to time-shift timing events. Set up is done via normal control system functionality.

All Timing Receivers will be handled as normal control system devices as any other accelerator equipment, thus standard device access methods will be used to e.g. set up trigger conditions.

## 5 Interfaces

[...]

### 5.1 Interfaces within the Control System

Database

Alarm System

LSA

UTC': The control system should also use UTC' as its absolute time. This would ease all timestamping related features like alarm logging, post mortem analysis, data correlation etc.

[...]

### 5.2 Interfaces within the Timing System

SNMP diagnostic device; possibly assignment in 5.1

WR connections copper/fiber; connection protocols, PTP, SyncE etc.

[...]

### 5.3 Timing Receiver Interfaces

Necessary interface description: How does the WR timing receiver/decoder communicate with front-end software? Hardware implementation? Ranging from simple event receivers to the front-end controller.

WR receiver/decoder <-> front-end software

- Front-end controller
- 

[...]

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<sup>7</sup> Not yet discussed on OHR, but from GSI point of view necessary.

### 5.4 Interfaces to the BuTiS System

Timing receivers have to create events for the rf components with a well-defined reference (phase) to  $T_0'$ . Therefore the result of the BuTiS delay compensation measurement must be known to the timing system.

In order to achieve this the  $T_0'$  clock from a BuTiS receiver will be provided to the timing master. The timing master itself will also be connected to some GPS (and/or Galileo) UTC receiver and will use the  $T_0'$  clock to change its received UTC time to  $UTC' := UTC + \delta t$ .  $UTC'$  will then be the master clock for the whole timing system.

Since  $\delta t$  is smaller than the time between two  $T_0'$  clocks, knowledge of  $T_0'$  is sufficient to calculate and distribute  $UTC'$ .

However, for the timing system it is desirable to receive not only the  $T_0'$  clock but also  $T_0$  and  $\delta t$  from the BuTiS system. Detailed interface definition will be discussed in time.

It is important to note that the timing events have to be sent and executed in conformance with the clock raster defined by  $T_0'$ . Therefore the granularity windows start (and necessarily also its end) will coincide with a  $T_0'$  clock.

In Figure 5 the correlation between the timing system and BuTiS is shown.

Correlation between the rf BuTiS system and the timing system at FAIR

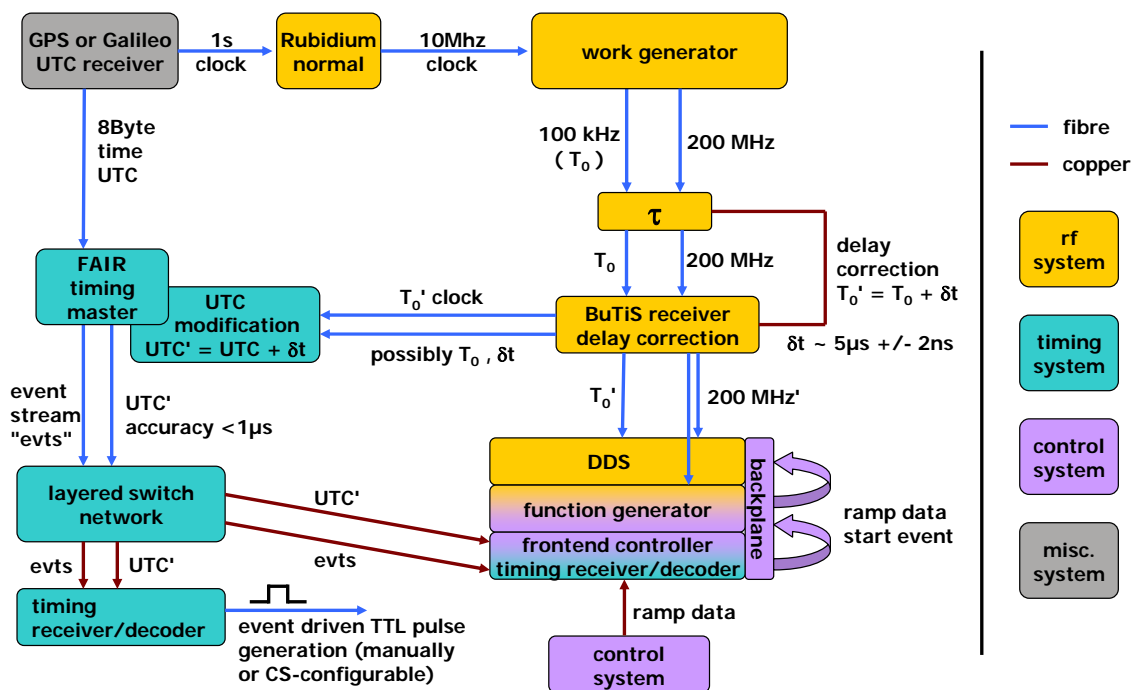


Figure 7 – Correlation between the timing system and BuTiS

### 5.5 Interfaces to the Beam Diagnostic System

Could be included in chapter 5.3  
 [...]

### 5.6 Interfaces to further Systems

The timing system will be closely coupled to the facilities interlock system. Perhaps the interlock system will even use the timing system for soft interlock handling. A possible realization scenario is shown in Figure 6.

## Interlock System

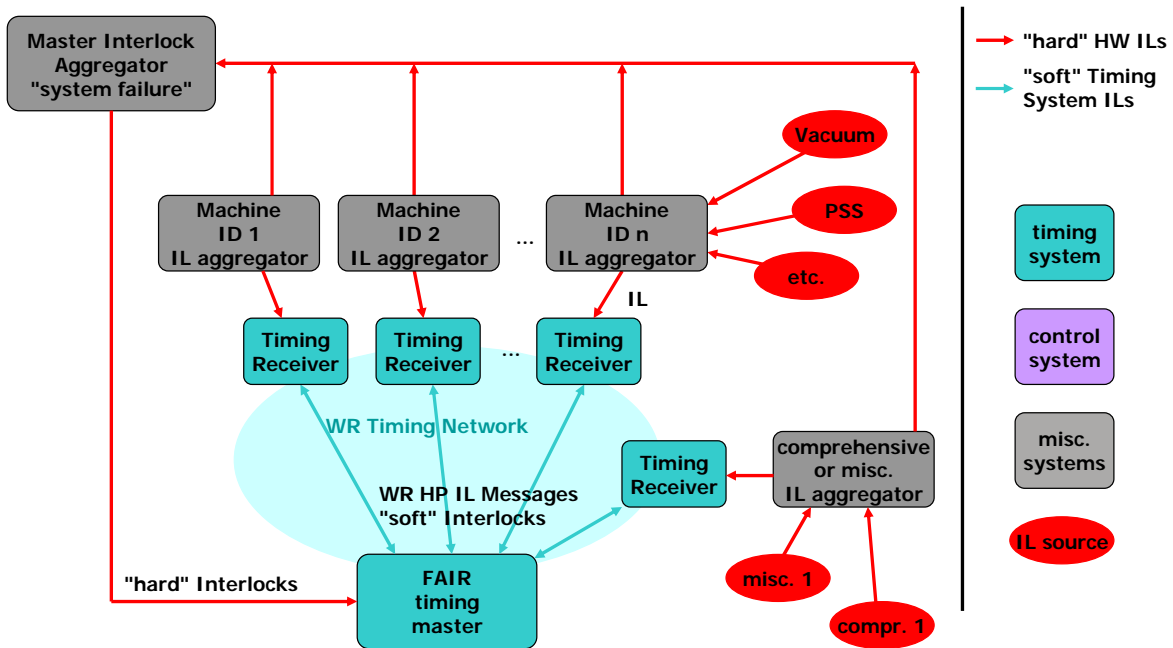


Figure 8

## 6 Requirements to Control Systems Database

The following timing system internal information have to be stored, written and read by the timing system to/from some central database:

- Life information about the general topology including all WR devices and its individual states. This includes IP/MAC addresses, port connections, device properties/set values, error counters, all SNMP data etc. Hold-back time and update frequency of status information are not yet defined.
- Software and firmware of all connected WR devices that are capable of remote updates; possibly file links are to be favored.
- Timing master settings
- ...

The following information has to be exchanged between GMT and the control system; most probably all of it via a database since the information also has to be stored:

- Machine event tables
- Interlock condition masks
- ...

## 7 Open Questions / Issues

- Timing master check upon validity of events? e.g. that different beams handled in parallel will not use overlapping areas of the facility (--> colliding beam experiments)
- base period (1 $\mu$ s) needed for the timing master / central master clock ? --> sync. information exchange at central master clock ticks? --> only reasonable with real delay compensation?
- delay compensation in TRs? Not necessary due to gran. window concept, but still...?
- local clock question
- Transparency to normal network / PTP functionality for non-WRs
- ...