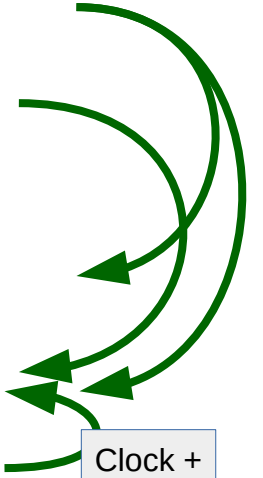
Time protocols

Protocol	DC bal.	PLL	Medium	Transmit	Receive	Encoding	Record	Rate	WRT-CLK	Future
White rabbit	Y	Y	RX+TX (Fiber)	Spec. HW	Spec. HW	Ethernet, 8b10b		1.25 GHz		“Gold standard”, Reference
Ratatime	Y		Any*	FPGA	FPGA	Self-align pattern		1 – 10 MHz	Out	Deprecate
Heimtime			Any*	FPGA	PC **(complex)**	Periodic + data	Y	200 – 400 Hz, varying	Out	Deprecate
Rataclock PLL	Y	Y	Any*	FPGA	FPGA	Clock w. PWM data		> 5 MHz	Out	
Rataclock slow	Y	(Y)	Any*	FPGA WR-LM32	FPGA	Clock w. PWM data		1 – 10 MHz	Out	
Heimtime II			Any*	WR-LM32 FPGA	PC FPGA	Periodic + data	Y	10 Hz – 100 kHz		FPGA versions
Clock + “Schakel”	Y + N	Y	2x LVDS	FPGA	FPGA	Clock / Time data		Clock: 200 MHz **50 MHz** @ 100 kHz	In	
Clock + reset	Y + N	Y	2x Any*	(FPGA)	(FPGA)	Clock / **Reset**				DO NOT USE !



Clock + HT II

Silent drift

Own time

Not really a timing protocol. Mentioned for completeness. “Androm till skräck or varnagel.”

For good continuous monitoring: FPGA decoder

Suitable for DAQ recording

DC balanced: Fixed long-term average of 0 and 1 signal.
PLL: PLL clock recovery.
1-wire: Protocol uses one signal. (Any medium.)
Transmit: Code for transmitter.
WR-LM32 is softcore in WR modules.
Receive: Code for receiver.
Record: Suitable for DAQ recording. (Low rate.)
Rate: Approximate signal rate / bandwidth.
WRTCLK: Handled by WRTCLK Exploder gateware.

* Any = NIM, ECL, LVDS, … Fiber for DC-balanced.

White text: Dev/future

Clock and time distribution