A FPGA/Labview-based Data Acquisition System for Microcalorimeters

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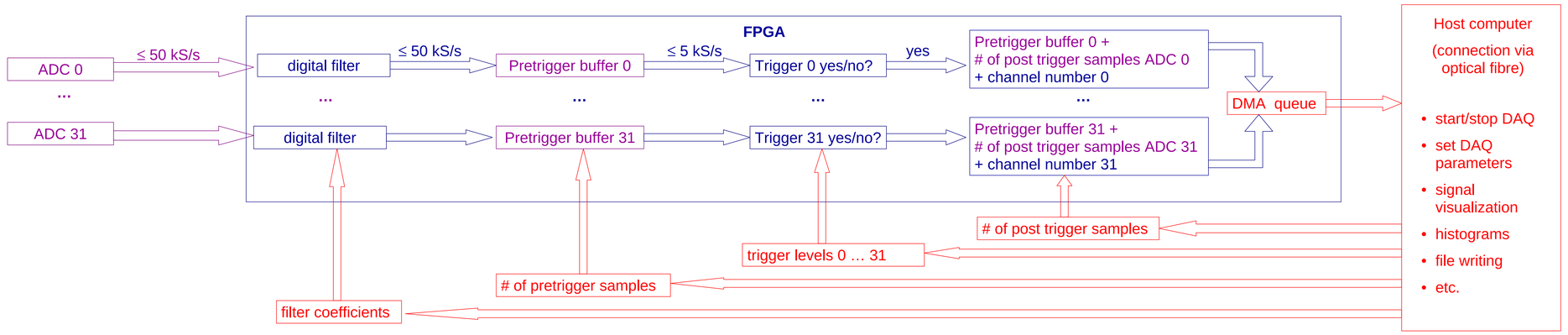
Motivation

High-resolution X-ray spectroscopy has become a versatile tool in atomic physics experiments with heavy ions: In first test experiments for the precise determination of the 1s Lamb Shift in hydrogen-like lead ions, good results have been obtained [1]. In these first experiments, a test array with 3 pixels consisting of silicon thermistors with lead absorbers has been used. To improve the statistical precision, a complete array with 32 pixels has since been prepared and tested in a channel-by-channel approach. To read out 32 channels simultanously, a new DAQ system has been developed.

[1] V.A. Andrianov et al., AIP Conf. Proc. 1185, 99 (2009))

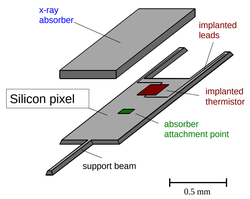
Schematic Setup



Detector Layout

thermistor array:

- developed and fabricated by Madison / Goddard group
- 36 pixel detector array
- 2 mm x 0.5 mm pixels



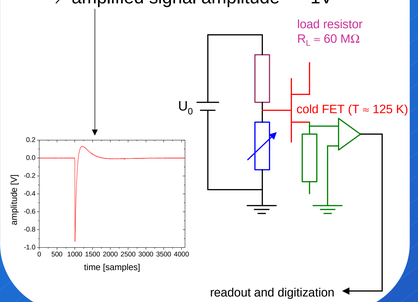
absorbers:

- optimized for 50-100 keV X-rays
- high Z material: Pb, Sn
- absorber thickness: 50 µm

readout scheme:

- thermistors coupled to cold JFETs
- voltage signal sent to preamplifier @ 300 K
- readout and digitization

→ amplified signal amplitude ~ –1V



Hardware

for 32 channels

8 NI9239 4-channel ADCs

- resolution 24 bit
- ≤ 50 kS/s per channel
- built-in anti-aliasing filter

2 NI 7813R FPGA cRIO-Controller

- 40 MHz frequency
- 216 kByte embedded block RAM

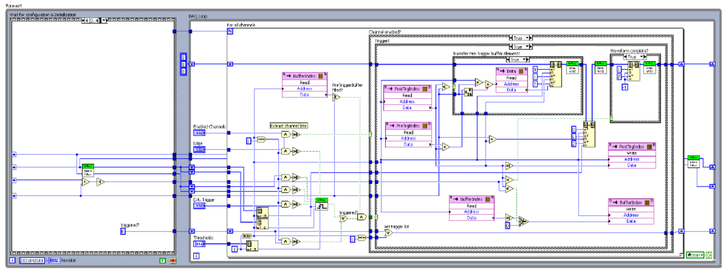
1 NI MXI8336 module

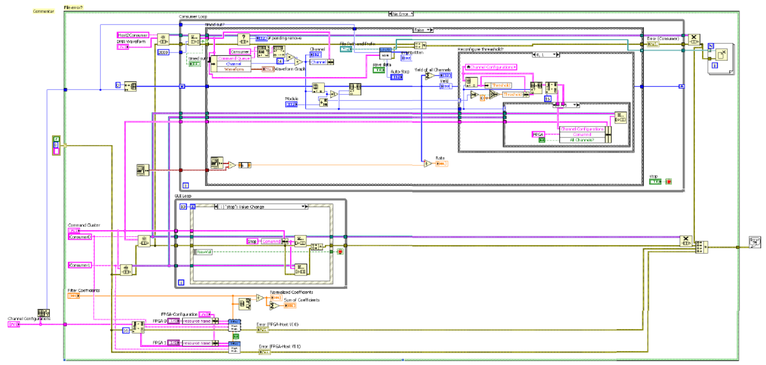
- connection to host PC via fiber-optic cable
- data rate up to 132 MByte/s

costs ~ 600 €/channel

Software: Labview Virtual Instruments

FPGA VI: block diagram





Host PC vi: block diagram

FPGA VI:

- data from ADC stored in a pretrigger circular rollover-buffer (size limited by onboard block RAM)
- independent triggering for each channel (internal by trigger level or external by TTL)
- first-stage digital filter (non-recursive weighted 10:1 averaging), filter coefficients provided by host PC VI

Host PC VI:

- free choice of number of pretrigger and post trigger samples, limited by FPGA onboard block RAM
- independent choice of trigger level for each individual channel
- automated recording of noise signals: Trigger level is set to 0 for each channel individually after n signals (n = 0, 1, 2, …)
- signal visualization and recording
- integration of further analysis steps possible
- modular and easily extendable to a larger number of FPGA controllers

Investigation of performance is currently underway.

For further details, please visit also http://wiki.gsi.de/cgi-bin/view/NIUser/XRayBolometerReadout .