# COMMON MODULES PROGRAMMING PROCEDURE STEP BY STEP

## Contents

# 1 Introduction

This document describes step by step the programming procedure for all the ACU System common modules:

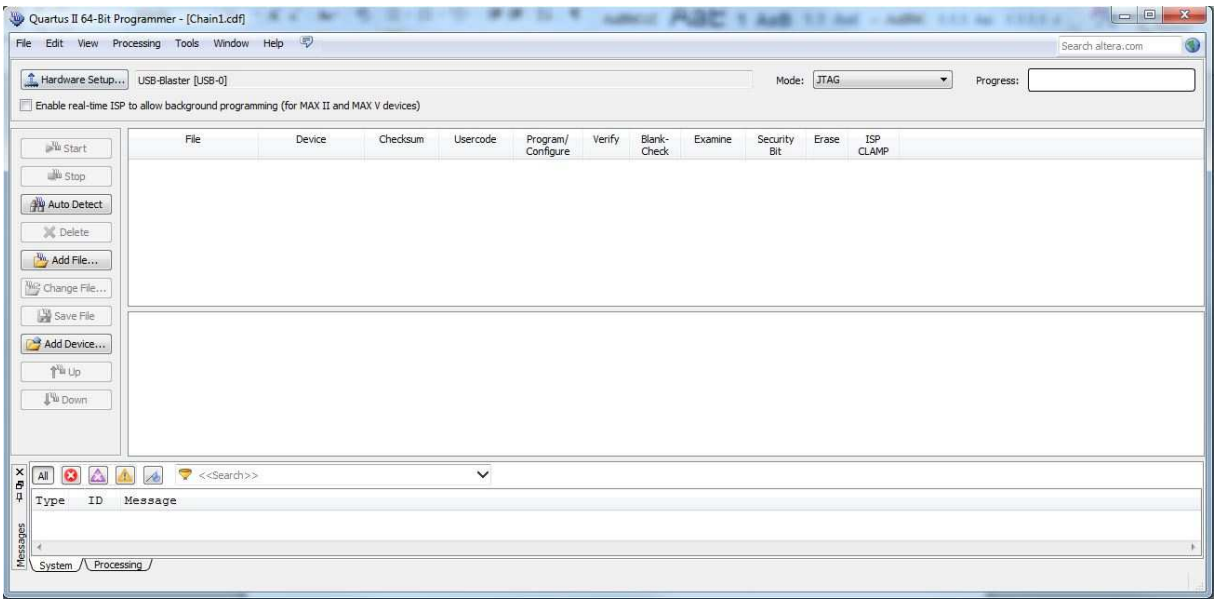
- ACU_40xInterlock_Board
- ACU_ADC_DAC_IO_Module
- ACU_ADC_DAC_IO_Module_VerII
- ACU_ADC_Module_II
- ACU_AnalogInterlockModule
- ACU_ICM
- ACU_MFU_TFTFrontPanel
- ACU_WaterInterlockAndControlModule _II

For the excluded ones (the MFU, SR Module and the Parallel Feeder) two dedicated documents will be provided.

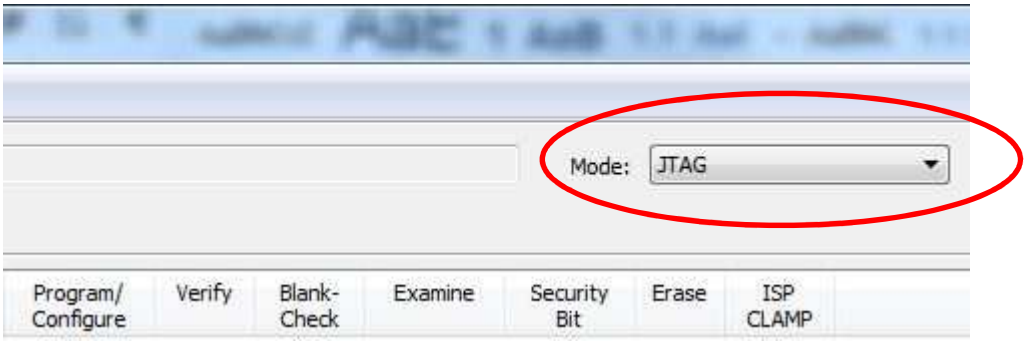
## 2 Steps

1. Connect USB Blaster cable to the JTAG connector.

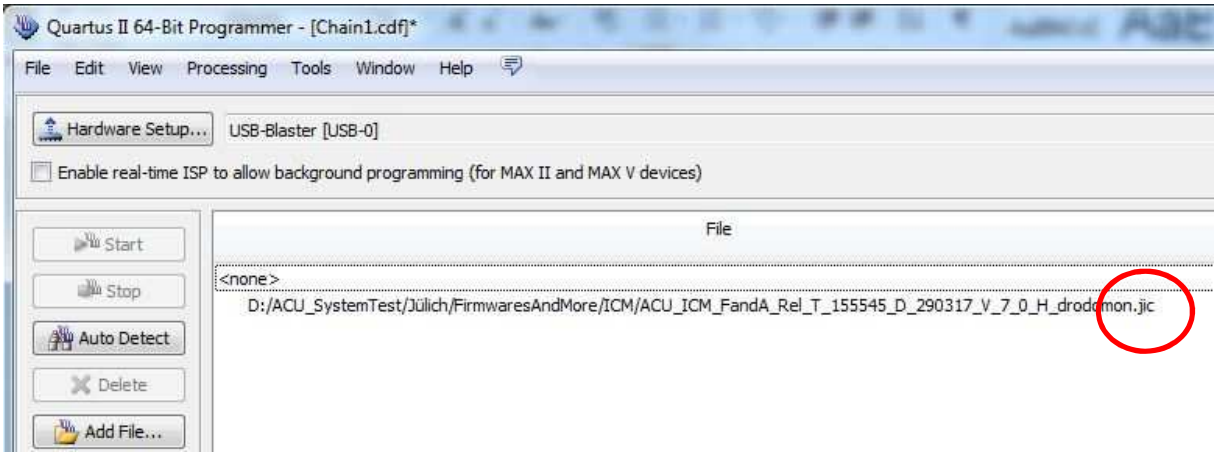
2. Open Quartus Programmer tool(quartus_pgmw.exe. It is located in the Altera installation folder (altera\13.1\quartus\bin).



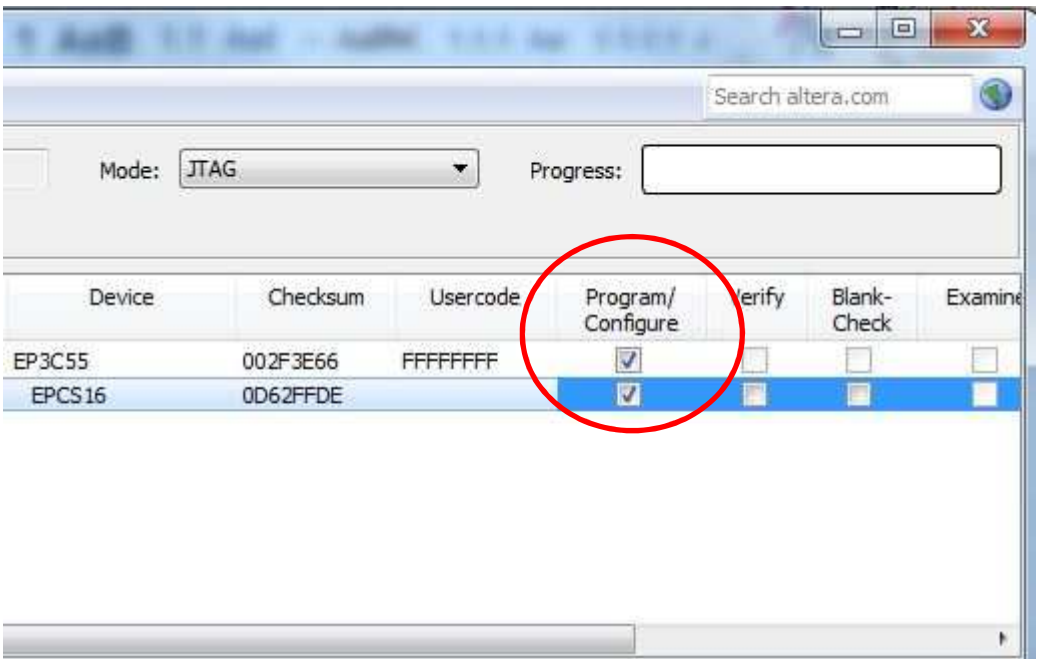

3. Check if the programming modality is JTAG, otherwise select it.



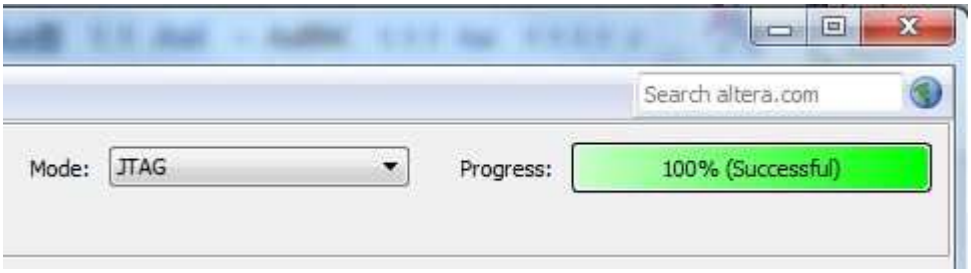

4. Push *Add File...* button and select the firmware file with .jic as extension. Below there is, only as example, the ICM Firmware file selected. Please select the appropriate file compliant with the FPGA to configure.



5. Check the second from the top *Program/Configure* check box; the first will be automatically checked.



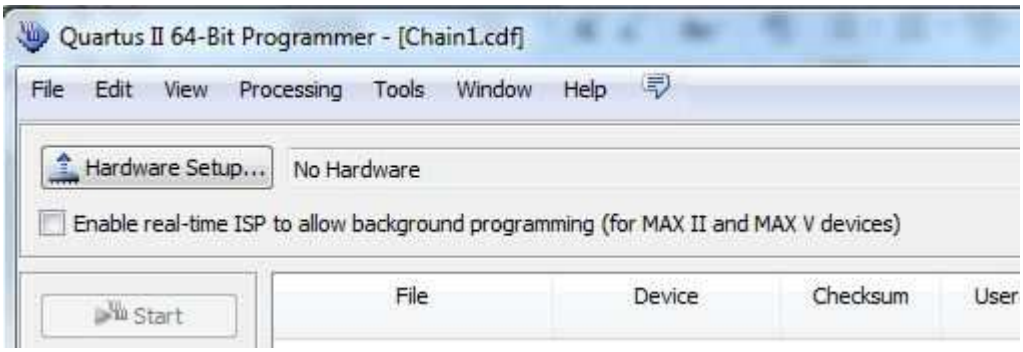

6. Push *Start* button and wait till the progress bar reaches the 100% and the *Successful* label appears in it (as in the picture below).



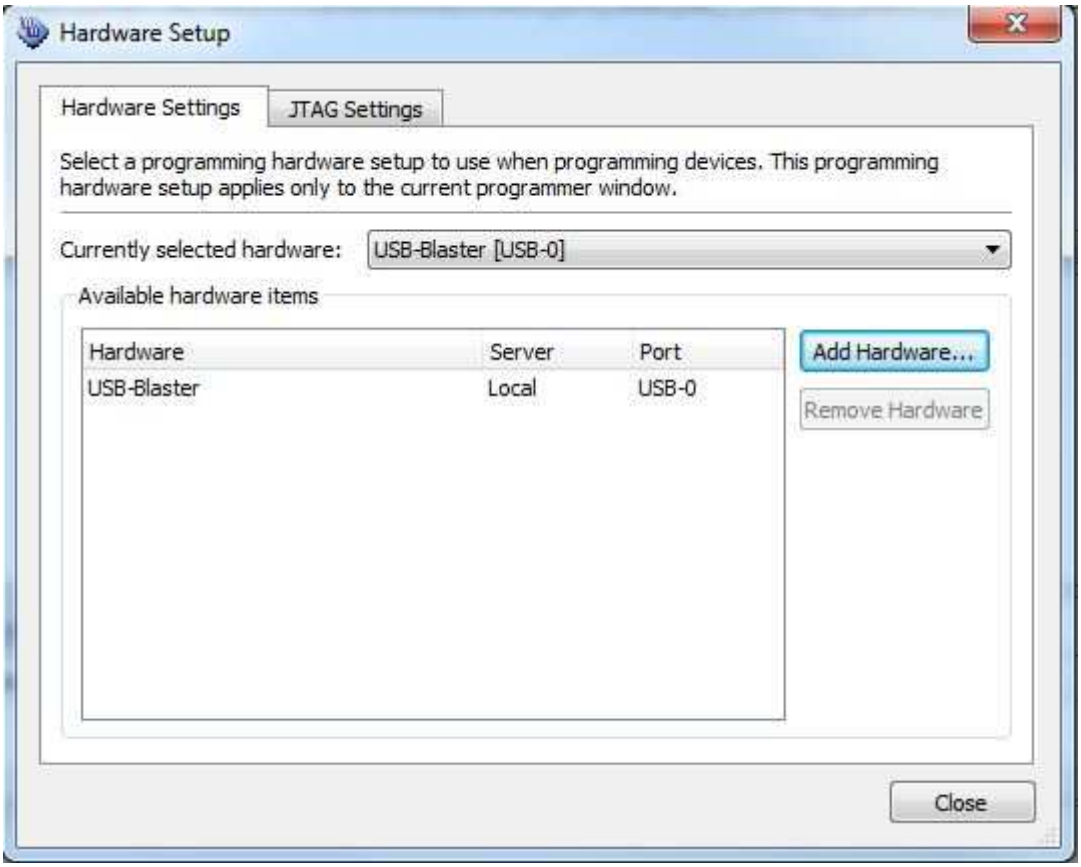

7. Power OFF and ON the board in order to start the new downloaded Firmware

# 3 COMMON PROBLEMS DURING THE FW DOWLOADING:

1. If pushing the *Start* button has no effect, please check if the USB Blaster hardware is recognized by the Quartus programmer. If not, *No Hardware Selected* should be displayed on the upper window side near to the *Hardware Setup* button as shown below.




In this case check first of all if the USB Blaster and cable are connected to the PC, after that click the *Hardware Setup* button.




In the Currently selected list select USB-Blaster as shown above, click the *Close* button and try again to program the FPGA.

2. If the progress bar becomes red and inside it is written *Failed,* the causes can be several. Below there are reported the two most common:

    a. The wrong .jic file is selected and for this reason there is no matching between the FPGA Hardware and Firmware.
    b. The EPCS memory is broken or defective.

    In these cases, please contact the supervisor.