Four Channel QFW Modul
Preliminary Datasheet

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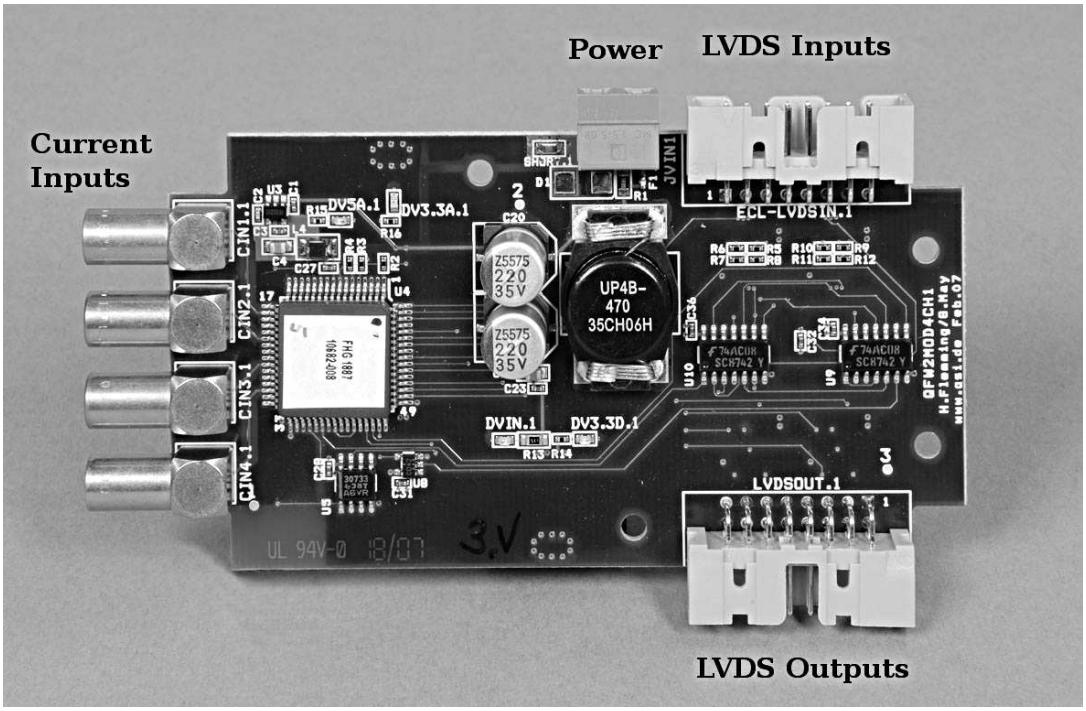

1 Introduction

The four channel QFW modul is a ready to use high dynamic range current to frequency converter modul. It is based on the QFW II ASIC, designed by the GSI EE department. Main features are:

- Single Power Supply from 5.2 V to 7 V
- Low power consumption
- Positive and negative input currents programmable
- Programmable resolution of 0.25 pC/pulse or 2.5 pC/pulse
- Overcurrent detection
- LVDS digital outputs
- Digital inputs compatible to LVDS and ECL

2 Connectors

2.1 Power Supply

For power supply a two pin Phoenix power connector is used placed at the right side of the pc board. The internal voltage regulators are able to cope with an input voltage range from 5.2 V up to 7 V. The input current of the four channel QFW modul is nearly 300 mA.

2.2 Input current

For the input current which has to be measured four Lemo type coaxial connectors are placed on the top side of the pc board. These connectors have a common ground which is connected to the negativ power supply pin.

2.3 Digital IO

Pins				active
Out1+	1	2	Out1-	high
Out2+	3	4	Out2-	high
Out3+	5	6	Out3-	high
Out4+	7	8	Out4-	high
Err1+	9	10	Err1-	high
Err2+	11	12	Err2-	high
Err3+	13	14	Err3-	high
Err4+	15	16	Err4-	high

Table 1: connection scheme of the digital output connector

Table 1 shows the connection scheme of the digital output connector which is placed on the right side of the modul. All signals are LVDS signals. *Out1* to *Out4* are the frequency outputs of the four converter channels. *Err1* to *Err4* are the error flags which will go into active stage when the input current exceeds the upper limit.

Pins				active
ConfEn+	1	2	ConfEn-	low
NC	3	4	NC	
QFWReset+	5	6	QFWReset-	low
Reset+	7	8	Reset-	low
RE1+/SDC+	9	10	RE1-/SDC-	high
RE2+/SDA+	11	12	RE2-/SDA-	high
RE3+/LE+	13	14	RE3-/LE-	high
RE4+/NC	15	16	RE4-/NC	high

Table 2: connection scheme of the digital input connector

In table 2 the connection scheme of the digital input connector is shown which is placed on the left side of the modul. All inputs are equipped with LVDS receivers with a common mode range from -4 V to +5 V. Due to the large common mode range also driving the inputs with ECL signals is possible. The differential inputs are terminated with 100 Ω resistors.

ConfEn sets the device into the configuration mode. If it is activ pins 9 to 16 are used as *SDA*, *SDC* and *LE* inputs. In the other case these Pins are used as Error-Reset inputs *RE1* to *RE4*.
QFWReset resets only the four converter channel without changing the modul configuration. In contrast the *Reset* input sets the modul configuration to a default configuration. For a complete initialization of the QFW2-ASIC both reset signals have to be set to active level.
RE1 to *RE4* are the error resets which resets the overcurrent error flags *Err1* to *Err4*. *SDA*, *SDC* and *LE* are used as a three wire serial bus to configure the QFW modul.
ConfEn, *QFWReset* and *Reset* are low active in contrast to all other in- and output signals which are high active.

3 Operation

3.1 Power up

After switching on the power supply an internal power up reset generator initializeses the QFW modul. The modul configuration is in default mode.

3.2 Configuration

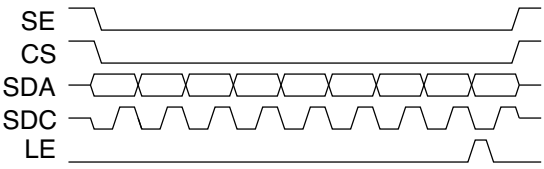

Figure 1: timing diagram of serial configuration at the input of the QFW2-module. SE and CS are connected to the *ConfEn* input

To invoke the configuration mode *ConfEn* input has to be set to active level (low). The timing of the serial configuration is shown in figure 1. Serial data has to be connected to *SDA* input (pin 11/12). Each data bit beginning with bit 7 is shifted into the serial receiver on the positive edge of *SDC* (pin 9/10).

When a byte is completed, it can be written into the configuration registers by the positive edge of *LE* (pin 13/14). Register 0 is written with the first positive edge of *LE* after the configuration mode is invoked.

After changing the configuration a *QFWReset* has to be invoked to reinitialize the converter channels. Alternatively it is also possible the set the *QFWReset* signal active during the whole programming phase.

3.2.1 Configuration Register

The QFW II ASIC on which the modul is based has ten 8 bit configuration registers, numbered from 0 to 9. During configuration data transfer register 0 is written first, register 9 is written last.

Register 0 is the main configuration register. The bits are used as following:

Bit 7: PosNeg If PosNeg is set to one, the charge to frequency converters are sensitive for positive currents. In the other case, negative currents are measured.

Bit 6: CSel With CSel the value of the integration capacity can be choosen. If this bit is set to zero, an integration capacity of 2.5 pF leading to a charge resolution of 0.25 pC is choosen. If it is set to one, the integration capacity is ten times higher. Due to the lower charge resolution of 2.5 pC per pulse, the maximum input current increases by one order of magnitude.

Bit 5: Unused

Bit 4: Cnt_Enable To enable the onchip readout counters this bit has to be set to one. If it is set to zero, the counters are disabled. The internal readout counters of the QFW II ASIC can not be used on the four channel QFW modul so this bit must be set to zero.

Bit 3: GC1, Bit 2: GC0 With the Gate Control bits the readout periode time is set. With the four channel QFW modul the internal readout system can not be used.

Bit 1: ROC1, Bit 0: ROC0 With the Readout Control bits the data transfer rate during data pushing is set. With the four channel QFW modul the internal readout system can not be used.

After reset or power up, all bits of register 0 are set to zero.

Register 1 is the chip-ID register. This ID is only useful in the internal QFW II readout mode which can not be used on the modul.

Register 2 and 3 are the data registers of the $\mathrm{V_{zero}}$ reference voltage DAC. Register 2 contains bits 8 and 9, register 3 contains bits zero to seven. After reset $\mathrm{D_{zero}}$ is set to 150_d or 00.10010110_b.

Register 4 and 5 are the data registers of the $\mathrm{V_{low}}$ reference voltage DAC. Register 4 contains bits 8 and 9, register 5 contains bits zero to seven. After reset $\mathrm{D_{low}}$ is set to 250_d or 00.11111010_b.

Register 6 and 7 are the data registers of the $\mathrm{V_{high}}$ reference voltage DAC. Register 6 contains bits 8 and 9, register 7 contains bits zero to seven. After reset $\mathrm{D_{high}}$ is set to 750_d or 10.11101110_b.

Register 8 and 9 are the data registers of the $\mathrm{V_{full}}$ reference voltage DAC. Register 8 contains bits 8 and 9, register 9 contains bits zero to seven. After reset $\mathrm{D_{full}}$ is set to 750_d or 10.11101110_b.

3.3 Measurement

After configuration and before starting any measurement a positive signal of minimum 100 ns on *QFWReset* should be invoked to initialize the converters. Afterwards on the Output *Outn* a pulse rate can be observed which is proportional to the input current I_n. It is the users task to count these output pulses to determine the charge flow on the input.

If the input current exceeds the upper current limit of the converter an internal error register is set. This register stops operation of this converter channel and resets it immediatly. To reset this error register the user has to impress a positive signal on the according *REn* input. After this the error register is cleared and the converter channel starts to operate again.

4 Static and dynamic parameters

4.1 Static parameters

4.1.1 Power Supply

Parameter	min	typ	max	Unit
VDC	5.2		7	V
IDC		300		mA
Total Powerdissipation	1,5		2,1	W

4.1.2 Logic Level

Parameter	min	typ	max	Unit
Magnetude of differential Input	0.1		2.5	V
Common mode of diff. Input	-4		5	V
Differential output voltage magnetude ($R_L = 100\Omega$)	247	340	454	mV
Common mode ouput voltage	1.125	1.2	1.375	V

4.2 Dynamic parameters

4.2.1 Converter characteristics

Parameter			min	typ	max
Charge resolution	$C_{Int} = 2.5$ pF	pC	0.237	0.241	0.245
	$C_{Int} = 25$ pF	pC	2.35	2.40	2.43
I_{max}	$C_{Int} = 2.5$ pF	μA		13	
	$C_{Int} = 25$ pF	μA		130	
I_{leak}	negative Currents	pA	2	3.5	5.5
	positive Currents	pA	-0.5	-0.3	-0.1
Temperature coefficient	$C_{Int} = 2.5$ pF				
	$C_{Int} = 25$ pF				
Pulse width		ns		7.4	

Current Range with integral nonlinearity better than 1 % or 0.1 %.

Current Direction	Charge Resolution	≤ 1 %		≤ 0.1 %	
		min	max	min	max
Negative	Low	20 pA	10 μA	300 pA	200 nA
	High	25 pA	2,2 μA	250 pA	2,5 nA
Positive	Low	1 pA	10 μA	20 pA	250 nA
	High	3 pA	2 μA	100 pA	50 nA

Integral nonlinearity in the current range from 50 pA to 1 μA and 50 pA to 10 μA

Current Direction	Charge Resolution	50 pA to 1 μA	
		min	max
Negative	Low	-0,3 %	+0,2 %
	High	-0,5 %	+0,5 %
Positive	Low	-0,15 %	+0,1 %
	High	-0,6 %	+0,2 %

Current Direction	Charge Resolution	50 pA to 10 μA	
		min	max
Negative	Low	-0,35 %	+0,2 %
	High	-4 %	+0,5 %
Positive	Low	-0,4 %	+0,07 %
	High	-4,5 %	+0,2 %

4.3 Converter characteristics

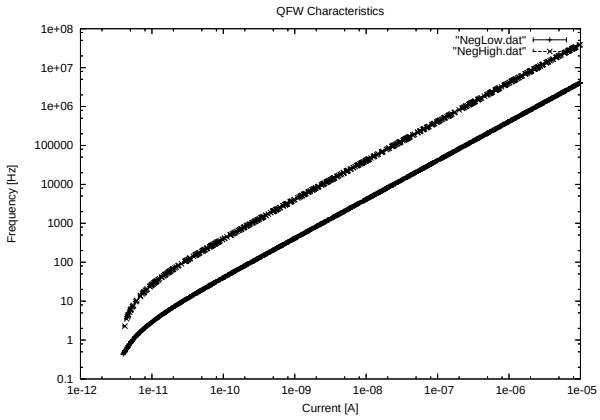

Figure 2: Converter characteristics for negative currents

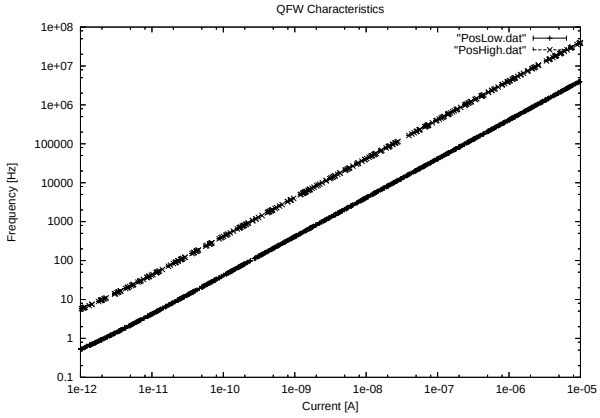

Figure 3: Converter characteristics for positive currents

Figures 2 and 3 show measured converter characteristics for negative and positive currents over seven orders of magnitude in current. In both cases the output frequency of the converter is plotted over the input current in low and high resolution mode.
To estimate the behavior at very small currents the current range up to 10 pA is plotted in figures 4 and 5. One can see that the characteristics do not cross the origin of the axis in both cases due to leakage currents. In case of negative currents a minimum input current in the order of 3 pA is needed to genarate an output signal. In case of positive currents a dark rate in the order of 1 Hz is caused by leakage currents. By substraction of this dark rate measurements of positive currents below 100 fA are possible.

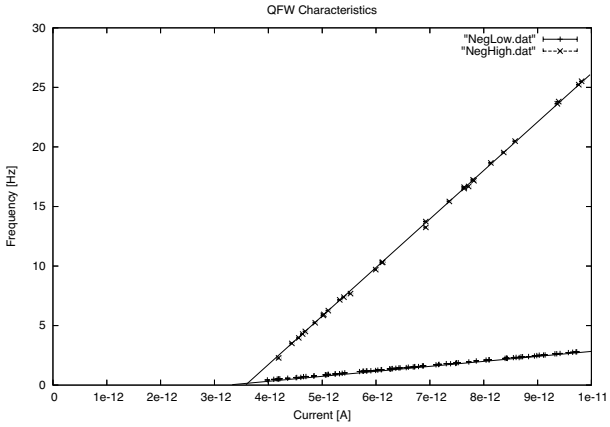

Figure 4: Converter characteristics for small negative currents

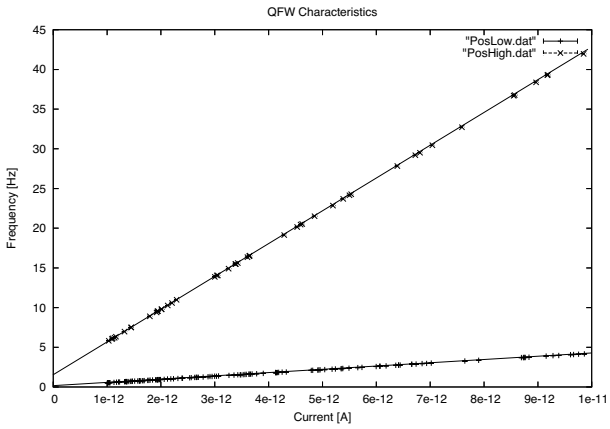

Figure 5: Converter characteristics for small positive currents

To get an information about the linearity of the current to frequency converter in figures 6 to 9 the relative deviation of the measured frequency from linear behavior is plotted over the input current. Figures 6 and 7 show this for negative currents in low and high resolution mode. At very low currents a large statistical spread due to a very low output frequency and limited measuring gate time are observable. Internal delays of

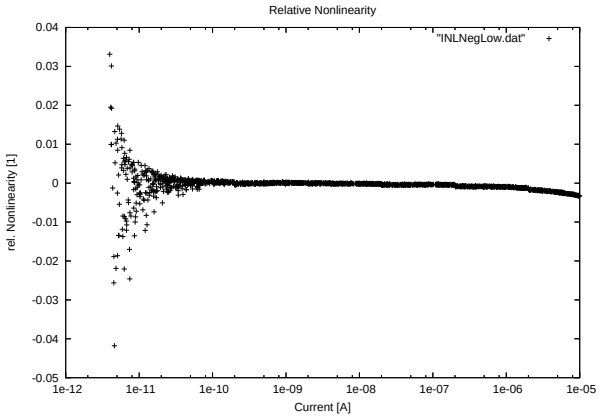

Figure 6: Relative nonlinearity for negative currents in the low resolution mode

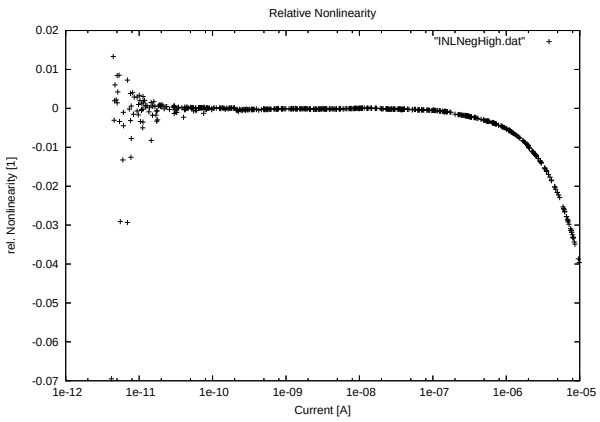

Figure 7: Relative nonlinearity for negative currents in the high resolution mode

the comparator, counter and DAC in the converter cores lead into a small dead time during overtaking operation from one converter core to the other. As this dead time is constant and the measuring time of one converter core decreases with increasing frequencis a charge loss due to this dead time becomes more significant at higher output frequencies. This leads into a decline of the output frequency starting at currents between 100 nA and 1 μA as it is visible in figures 6 and 7. As in high resolution mode the output frequency is ten times higher here the effect is more significant. In figure 8 and 9

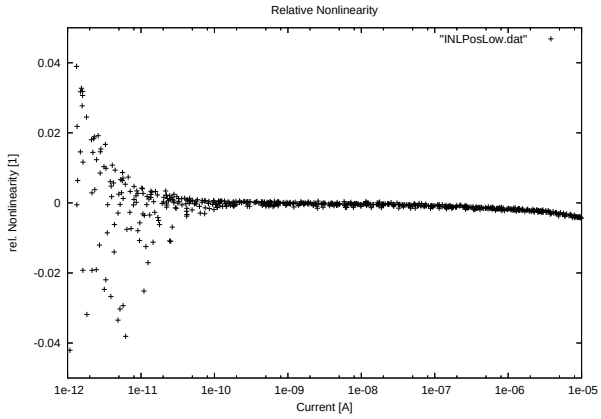

Figure 8: Relative nonlinearity for positive currents in the low resolution mode

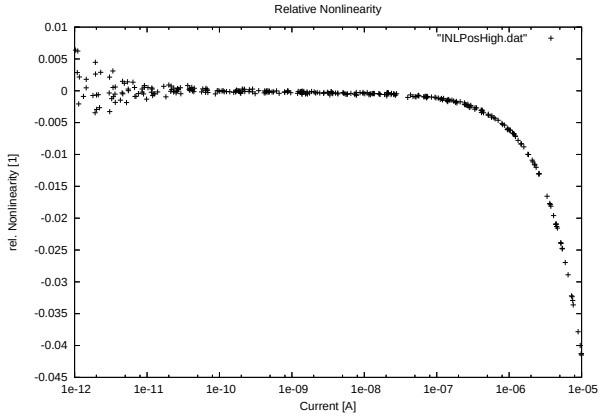

Figure 9: Relative nonlinearity for positive currents in the high resolution mode

the same mesurements are shown for positive currents. In all cases the plots show the excellent linearity of the device over a very large dynamic range.