

Charge-Frequency-Converter (QFW) Test Board and Results

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Overview

GSI Beam Diagnostics department recently started investigations on an economic solution for profile grid electronics. The front-end amplifiers and control devices presently used are outdated, very expensive and important parts, like low noise amplifiers, have long delivery times and/or have been discontinued by the manufacturer.

For the FAIR beamlines, around one hundred profile grid systems will be needed. The QFW CMOS-ASIC (Charge-Frequency-Converter [1][3]), developed by the Experiment Electronics department (EE) is a very promising candidate for a new design of the profile grids, due to its high dynamic range without the need for any range switching.

After first tests with the 4-channel QFW module [2], it was decided to develop a new board, more related to practice and with additional electronic features (Fig. 1).

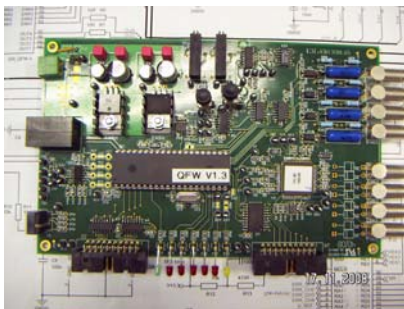


Fig. 1: New QFW-board with PIC micro-controller, display LEDs, current divider, LVDS-/LV-TTL-drivers.

Hard- and Software

The experimental board shown in Fig. 1 consists of:

- 4-channel QFW II
- current divider (for extended measuring range)
- LVDS- or LV-TTL outputs drivers
- power-supply for external devices (+3.3V/+5V)
- ICD-interface
- two precision voltage sources
- micro-controller Microchip® PIC 18FL4520
- several LEDs, hex-switch and two push-buttons

This board was designed in order to check the QFW in different operational modes, thus enabling measurements in the experimental areas of GSI. It was negotiated between Bio-Physics dept. and EE to add a selectable current divider onto the board, making it possible to measure currents up to 20 mA, of course dependent on the values of the circuit elements. Free-programmable LEDs, push buttons, a hex-switch and several I/O channels allow for adoption of the board to different measurement tasks.

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Output pulses and overload-bits are fed to their connector plugs through LVDS- or LV-TTL-drivers.

The micro-controller software was programmed in assembler via Microchip MPLAB®. The hex-switch allows changing range and polarity. After Power-On or Reset with the related buttons, the micro-controller transfers the necessary instructions to the QFW interface, whereupon operation starts.

Measurement Results

The QFW was tested under different conditions. At first the agreement with the results from the QFW datasheet and jitter behaviour was checked, and then tests under different ambient temperatures and different levels of X-radiation were carried out (see [4] for more information). A jitter around 0.1 ppt or better at each particular current value was detected by using an HP time interval analyser 5372A.

The linearity of the frequency outputs fulfils the requirements for future profile grid electronics. Also the frequency deviation between each channel and a reference signal was investigated. This deviation is better than 1 % Full Scale.

The temperature behaviour studies were performed in a climatic exposure cabinet. Many measurement series were done between 0°C and 50°C. The results show a deviation of 0.7 % only, with respect to the 20°C reference.

Presently, all these results show that the QFW ASIC can be used in a new design for profile grid electronics. Additional comprehensive tests are in progress.

Outlook

A new QFW board equipped with 8 ASICs will be developed in 2010, in collaboration with the EE department. This prototype will be controlled by an existing FPGA-I/O VME board (VUPROM).

A LabVIEW program will control the measurements. First beam tests of the prototype will be performed with a 2x16-wire profile grid in an experimental beamline at GSI. The board will also be used for further characterisation of the QFW ASIC.

References

- [1] H. Flemming, QFW II Preliminary Datasheet, GSI, 2008
- [2] H. Flemming, QFW Module Preliminary Datasheet, GSI, 2007
- [3] H. Flemming, E. Badura, A High Dynamic Charge to Frequency Converter ASIC, GSI Scientific Report, 2004
- [4] S. Löchner, Total Ionising Dose Studies of the QFW ASIC, GSI Scientific Report, 2009.