Radiation Studies on the UMC 180 nm CMOS Process at GSI

Sven Löchner, *Member, IEEE,* Harald Deppe, Holger Flemming

***Abstract*—GRISU test ASICs were irradiated with different types of heavy ions, fluences up to 10^{12} ions/cm^2 and with a LET in the range of 1 – 60 MeV cm^2/mg. Cross sections for SEU/SET were measured during the tests. Furthermore TID measurements were applied. Results on degradation and annealing are reported.**

I. Introduction

RADIATION damages to electronic components are an important issue for the future experiments at the new FAIR[1] accelerator facility. One of the preferred technology for ASIC developments is the 180 nm UMC CMOS process. In this regard the ASIC design group of the GSI Experiment Electronic department [1] has been launched a research project in 2007, including the development of an ASIC called *GRISU*. The main goal is the characterisation of Single Event Effects (SEE) and Total Ionising Dose effects (TID) on the 180 nm UMC process as well as the installation of a testing site for heavy ion irradiation at the GSI linear accelerator.

II. *GRISU* Test ASIC

Before starting the radiation studies a test chip on the UMC 180 nm CMOS technology was developed and submitted in 2008. The *GRISU* ASIC has a size of $1.5 \times 1.5\,\text{mm}^2$. It consists of test structures for SEE analysis (e.g. different D-flip-flop architectures, groups of inverters) and single basic transistors as well as two ring oscillators for TID measurements. Fig. 1 shows the layout of this test chip. In total 64 pads are located on the chip, clearly visible in the layout.

III. Single Event Effect Studies

Single Event Effect is the main generic term for effects in semiconductor devices triggered by the impact of ionising particles. Within the SEE there are more detailed types of effects. Of great interest for the future FAIR experiments are the so-called Single Event Upset (SEU) and Single Event Transient (SET) effects.

A good choice to test these effects is the irradiation of the semiconductor devices with heavy ions. Therefore the *GRISU* test chip has been particular designed to monitor these effects during irradiation.

For SEU testing two groups each consisting of four channels with up to 320 flip-flops cells were implemented on the test chip. Exemplarily the block diagram of one of these groups is shown in Fig. 2. Each of the eight channels vary either in layout modifications or in a different flip-flop architecture. An overview of the different flip-flop cells is given in Table I.

S. Löchner, H. Deppe and H. Flemming are with the GSI Helmholtzzentrum für Schwerionenforschung GmbH, Darmstadt, Germany

[1]Facility for Antiproton and Ion Research

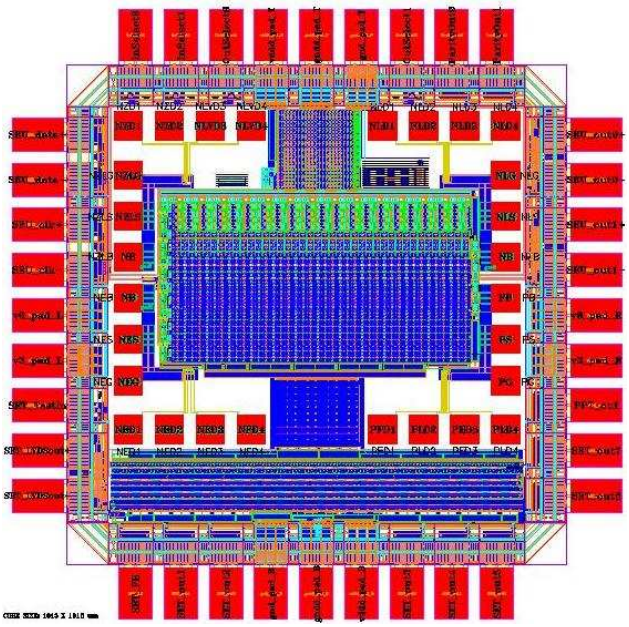

Fig. 1. Layout of the *GRISU* test ASIC.

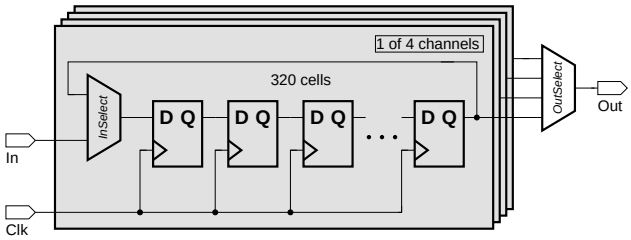

Fig. 2. Block diagram of a flip-flop group for SEU testing. Each group consists out of four channels with different flip-flop implementations.

Group	Flip-flop description	No. of cells
1	Std. D-type flip-flop	320
	D-type flip-flop with ”sized” transistors	320
	D-type flip-flop with internal buffers	320
	D-type flip-flop with short routing	160
2	Sense amplifier flip-flop with DICE structure (based on [2], [3])	160
	DICE cell based flip-flop (based on [3])	240
	D-type flip-flop with ”oversized” transistors	320
	D-type flip-flop with long routing	160

TABLE I
Overview of the flip-flop cells implemented for SEU testing

It is well known that the minimal LET for a SEU failure at a given node depends on the load respectively the capacitance of this node. Therefore a second block is implemented in

No.	W_{pmos} μm	L_{pmos} μm	W_{nmos} μm	L_{nmos} μm	C_{load} fF
1	0.48	0.18	0.24	0.18	1.24
2	0.96	0.18	0.48	0.18	2.39
3	1.92	0.18	0.96	0.18	4.68
4	2.88	0.18	1.44	0.18	6.99
5	5.76	0.18	2.88	0.18	13.87
6	11.52	0.18	5.76	0.18	27.62
7	23.04	0.18	11.52	0.18	55.91

TABLE II
DESIGN PARAMETER AND LOAD CAPACITANCE OF THE CMOS INVERTERS

No.	Q_{crit} fC	$\mathrm{LET}_{\mathrm{crit,d=2\mu m}}$ MeV cm^2 mg^{-1}	$\mathrm{LET}_{\mathrm{crit,d=0.5\mu m}}$ MeV cm^2 mg^{-1}
1	32	1.54	6.17
2	58	2.80	11.19
3	114	5.50	21.99
4	172	8.29	33.17
5	344	16.59	66.35
6	674	32.50	129,99
7	1346	64.90	259.60

TABLE III
SIMULATED CRITICAL CHARGE FOR THE IMPLEMENTED TEST STRUCTURES AND THE RESULTING EXPECTED CRITICAL LINEAR ENERGY TRANSFER

Beam parameters	
Available ions	all ions from Protons up to Uranium
Energy	11.4 MeV/AMU at exit window
Flux	$10^3 \ldots 10^{10}/(\mathrm{cm}^2 \cdot \mathrm{s})$
Beam size	50 mm in diameter
Location	radiation in air
Bunch length	up to 5 ms
Bunch frequency	max. 50 Hz

TABLE IV
BEAM PARAMETERS FOR THE LOW ENERGY TESTING SITE

the *GRISU* test chip for measuring the critical charge of the UMC 180 nm CMOS process for generating SET signals. It consists of seven different inverter chains differing in node capacitance and transistor size. The design parameter of the used transistors of these inverter chains a depict in Table II. From analogue simulations the theoretical critical charge is well known for each of these structures. According to

$$\mathrm{LET}_{\mathrm{crit}} = \frac{Q_{\mathrm{crit}} \cdot 3.6\,\mathrm{eV}}{e \cdot \rho_{\mathrm{Si}} \cdot d} \qquad (1)$$

and an assumption for the sensitive depth d of the charge collection the critical linear energy transfer $\mathrm{LET}_{\mathrm{crit}}$ can be calculated for each structure. Table III depicts the expected values of the critical charge as well as a realistic range for the critical linear energy transfer.

For a complete characterisation of both SEU and SET it is therefore necessary to measure the impact of ionising particles at different LET levels.

The irradiation tests of the *GRISU* chip were performed at the GSI heavy ion linear accelerator UNILAC[2]. An existing low energy testing site (X6) was chosen for the installation of the test setup. The beam parameter at the transfer point to the experimental site is depicted in Table IV.

[2]Universal Linear Accelerator

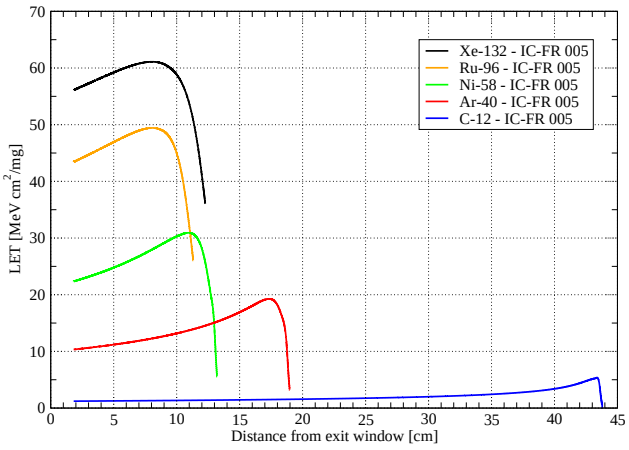

Fig. 3. Possible LET range for the available ions in 2008 and 2009 at the low energy testing site.

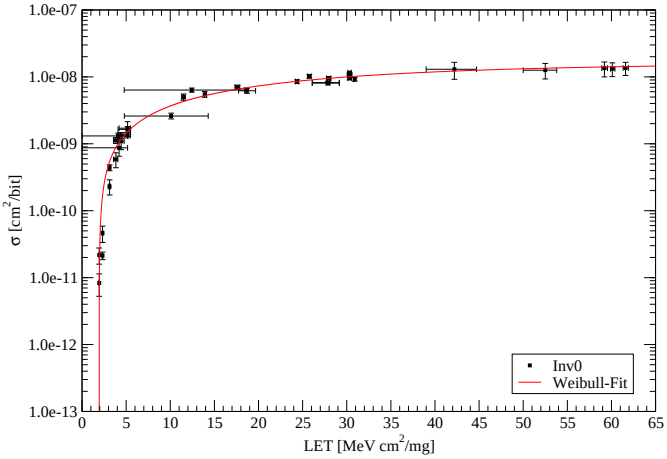

Fig. 4. Weibull fit of the SET cross section of a minimum sized inverter.

The coverage of the large LET range was obtained with different heavy ions. The beam energy is fixed during irradiation. Only the adjacent energy absorption in air after the exit window of the beam line is changeable during beamtime. An overview of the test setup position in beam and the resulting LET parameters for the available ions in 2008 and 2009 are shown in Fig. 3.

The measurement of SEU and SET events was done with a FPGA readout system. The irradiation where done in bunches of heavy ions with a bunch width of 1 ... 5 ms and a cycle time of 20 ... 200 ms. The resulting SET events were counted by the FPGA instantaneously during irradiation. In contrast SEU events in the flip-flops of the *GRISU* ASIC were read out and analysed in the gap between two bunches. Together with the known number of heavy ion particles per bunch the cross section of each test structure is calculated.

As an example the overall SET cross section versus LET is shown in Fig. 4 for a minimum sized inverter (No. 1). The critical linear energy transfer as well as the maximum cross section are extracted with a Weibull fit from the test results for each of the test structures. Table V summarizes all saturated cross section σ_{sat} and threshold $\mathrm{LET}_{\mathrm{crit}}$. The comparison between the simulated values (Table III) and the extracted measurement

No.	σ_{sat} cm^2/bit	LET_{crit} $MeV\,cm^2\,mg^{-1}$
1	$1.35 \cdot 10^{-8}$	1.939
2	$1.48 \cdot 10^{-8}$	1.945
3	$1.69 \cdot 10^{-8}$	2.021
4	$1.78 \cdot 10^{-8}$	1.953
5	$1.77 \cdot 10^{-8}$	1.900
6	$8.85 \cdot 10^{-9}$	1.899
7	$8.35 \cdot 10^{-10}$	1.898

TABLE V
EXTRACTED WEIBULL FIT PARAMETER FOR DIFFERENT TEST STRUCTURES

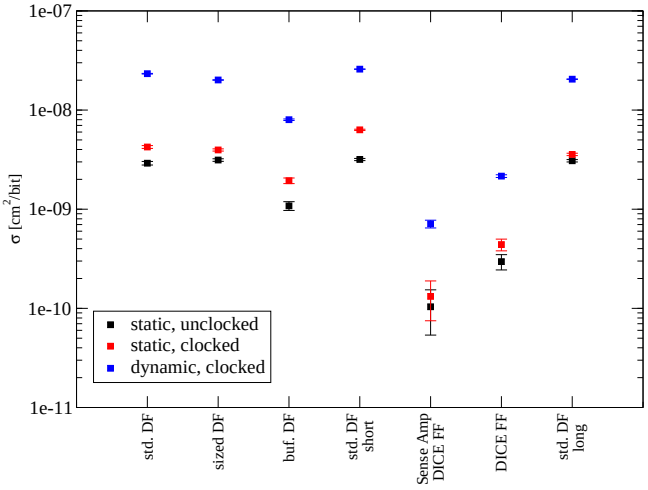

Fig. 5. Saturated SEU cross section of all flip-flop test structures. The applied clock frequency was 100 MHz.

values (Table V) shows a clear discrepancy between both data. Up to now this behaviour is not completely understood.

As the threshold LET_{crit} is nearly for all SET test structures, there is rapid drop of the saturated cross section for the larger test structures No. 6 and 7. To clarify and understand this decrease in sensitivity a so-called Single Heavy Ion Hit Microbeam test was performed. The testing method and first results are described in more detail in section IV.

Furthermore the sensitivity against SEU of all types of flip-flops has been tested for different operation modes (e.g. static unclocked, static clocked and dynamic clocked mode). A comparison of the saturated cross section of the 7 different flip-flop implementations is depict in Fig. 5. Both flip-flops with internal DICE structures respond more sensitive to SEU then expected from simulation. One possible explanation is a insufficient layout of the redundant transistors in these cells. A further microbeam test with a more accurate resolution might be helpful to understand this behaviour (cf. section IV and Outlook) .

IV. SINGLE EVENT EFFECT STUDIES WITH A SINGLE HEAVY ION HIT MICROBEAM

Briefly, the microbeam is situated at the end of the GSI heavy ion linear accelerator. The ions entering the microbeam line through object slits are focused down to a focal spot of about 500 nm in diameter by means of magnetic quadrupole lenses. Deflecting magnets, situated in front of the focusing

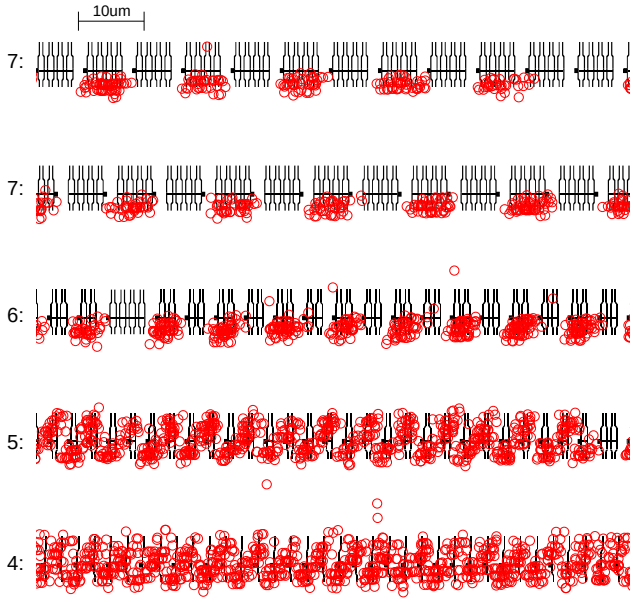

Fig. 6. Overlay of inverter chain test structure layout and position of SET events. The radius of the circle is equivalent to 3σ position accuracy or approx. 600 nm.

lenses, are used to move the beam spot in the focal plane. To ensure the irradiation with a preset number of particles, a fast electrostatic beam switch, situated in front of the object slits, is controlled by the hit detection system. Like all of the other heavy ion testing sites at GSI, the microbeam is able to focus ions from carbon to uranium with energies between 1.4 MeV/u to 11.4 MeV/u.

In May 2009 a GRISU chip was irradiated with a carbon microbeam with an energy of 4.8 MeV/u. This corresponds to an LET of approximately 2.25 $MeV\,cm^2\,mg^{-1}$. In total five different test structure areas were irradiated. The ASIC scanning area was $80 \times 80 \mu m^2$ for the first three tests respectively $20 \times 20 \mu m^2$ for last two tests.

As an example of these test results the layout overlay picture of the irradiated area and the observed SET events are shown in Fig. 6. Each red circle represents a SET event. The centre points to the measured origin by the microbeam DAQ system whereas the radius represents the 3σ position accuracy of 612 nm. For inverter chain 4 and 5 SET events were measured for NMOS transistors (lower layout part in each row) as well as for PMOS transistors (upper layout part). However for inverter chain 6 and 7 SET hits were only measured for NMOS transistors. The explanation for this is that the node capacitances of these PMOS transistors are larger compared to the smaller NMOS.

The first measurement show that the microbeam setup is a powerful tool for spartial resolving SEE investigations. However the resolution must be increased for closer investigations of the 180 nm process, especially for the study of the DICE structures.

V. TOTAL IONISING DOSE STUDIES

In 2008 a Total Ionising Dose (TID) test was performed at the X-ray irradiation facility of the Institute of Experimental

Number of chips	Dose rate [krad/h (SiO_2)]	Accumulated dose [krad (SiO_2)]
1	50	800
2	100	1000...1200
4	200	1600...2400
1	490	1500

TABLE VI
SUMMARY OF IRRADIATED *GRISU* CHIPS, DOSE RATES AND ACCUMULATED DOSES OF THE TID TEST.

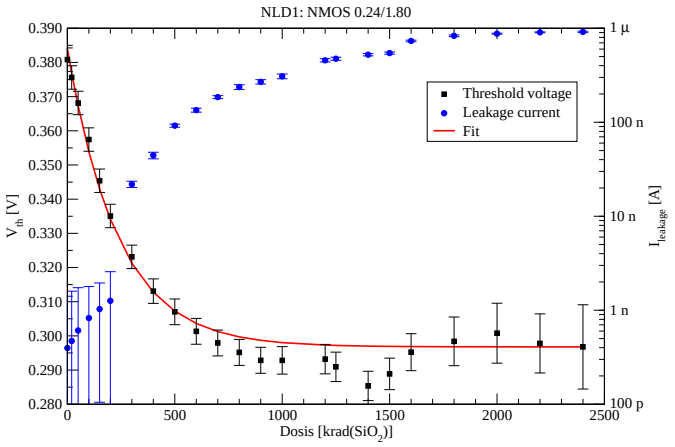

Fig. 7. Threshold voltage shift and leakage current of a single NMOS transistor (W/L = 0.24 μm/1.80 μm) for different dose levels.

Nuclear Physics (IEKP) [5] at Forschungszentrum Karlsruhe (FZK) [6]. In total 8 *GRISU* test chips have been irradiated. Table VI summaries the different dose rates and accumulated doses.

The transient and output characteristics of all 16 discrete MOSFET transistors as well as threshold voltage and leakage currents were measured for different accumulated dose levels.

Exemplarily the threshold voltage shift of a discrete NMOS transistor (W/L = 0.24 μm/1.80 μm) is shown in Fig. 7 for different accumulated dose levels. After total dose of 2.4 Mrad was exposed to an ASIC the measured leakage current for a single NMOS transistor increased up to 3 order of magnitude.

In addition the long term annealing characteristics were monitored. Annealing of the chips was immediately observed after the end of irradiation. After four weeks, keeping the chips biased and at room temperature, the leakage current for all transistors had settled back to the initial value. Finally, all chips showed a very good annealing performance

VI. SUMMARY AND OUTLOOK

A test ASIC for characterising the radiation hardness quality of the UMC 180 nm CMOS process was developed at the GSI ASIC design group. Furthermore a test site for heavy ion irradiation of complete ASIC chips as well as a heavy ion microbeam test site for single transistor irradiation have been set up at GSI. TID tests which have been done up to now have shown that this CMOS process is useful for future FAIR experiments. Especially the good TID annealing performance turned out to yield to no restrictions. SEE results have shown that maybe other techniques have to be used to decrease the sensibility to these events.

Further analysis of the test data will be done. In parallel a second microbeam test will be performed with a more accurate resolution of approx. 100 nm for SEE position detection. Then it will be possible to scan the digital DICE flip-flop cells and map the origin of SEU and SET sensibility.

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[5] Institute of Experimental Nuclear Physics (IEKP), University of Karlsruhe (TH), Karlsruhe, Germany http://www-ekp.physik.uni-karlsruhe.de
[6] Forschungszentrum Karlsruhe (FZK), Karlsruhe, Germany http://www.fzk.de

Sven Löchner received the Diploma and Ph.D. degrees in physics all from University of Heidelberg, Germany in 1999 and 2006. He was involved in the development of a radiation hard mixed-signal read-out chip for the LHCb experiment at the European Organization for Nuclear Research (CERN). His research interests include analogue ASIC designs, electronics, radiation effects and SEE testing methods with heavy ion beams.

Since 2006 Dr. Löchner is now working for the Experiment Electronics department at GSI Helmholtzzentrum für Schwerionenforschung GmbH, Germany.

Harald Deppe received his diploma degree in physics from the Ruhr-University Bochum, Germany in 1997. From 1998 to 2001 he was involved in the development of a read-out chip for the HERA-B experiment at Deutsches Elektronen-Synchrotron (DESY), Germany. From 2001 to 2004 he worked at the University of Heidelberg, Germany on the development of a radiation hard TDC ASIC for the LHCb experiment at the European Organization for Nuclear Research (CERN).

Since 2004 he is now working at the Experiment Electronic Department at GSI Helmholtzzentrum für Schwerionenforschung GmbH, Germany.

Holger Flemming was born in Wattenscheid, Germany in 1968. He received his diploma in experimental physics in 1996 from the Ruhr-University of Bochum for design and construction of the readout electronics for a miniaturised multi wire proportional chamber.

From 1996 he worked on design and realisation of a cluster trigger for the electromagnetic calorimeter of the CB-ELSA experiment based on cellular logic and received the Dr. rer. nat. degree from the university of Bochum in 2001.

Since 2002 he is with the Experiment Electronic Department at GSI Helmholtzzentrum für Schwerionenforschung GmbH, Germany where he is the head of the microelectronics group. His main interest is in analogue full custom designed microelectronics for particle physics detector readout.