Radiation Studies on the UMC 180 nm CMOS Process

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1 Introduction

Radiation damages to electronic components are an important issue for the future experiments at the new FAIR accelerator facility[1]. One of the preferred technologies for ASIC developments is the 180 nm UMC CMOS process. In this regard the ASIC design group of the GSI Experiment Electronic department has been launched a research project in 2007, including the development of an ASIC called *GRISU*. The main goal is the characterisation of Single Event Effects (SEE) and Total Ionising Dose effects (TID) on the 180 nm UMC process as well as the installation of a testing site for heavy ion irradiation at the GSI linear accelerator.

2 *GRISU* Test ASIC

Before starting the radiation studies a test chip on the UMC 180 nm CMOS technology was developed and submitted in 2008. The *GRISU* ASIC has a chip size of $1.5 \times 1.5\,\mathrm{mm}^2$. It consists of test structures for SEE analysis (e.g. different D-flip-flop architectures, groups of inverters) and single basic transistors as well as two ring oscillators for TID measurements. Fig. 1 shows the layout of this test chip.

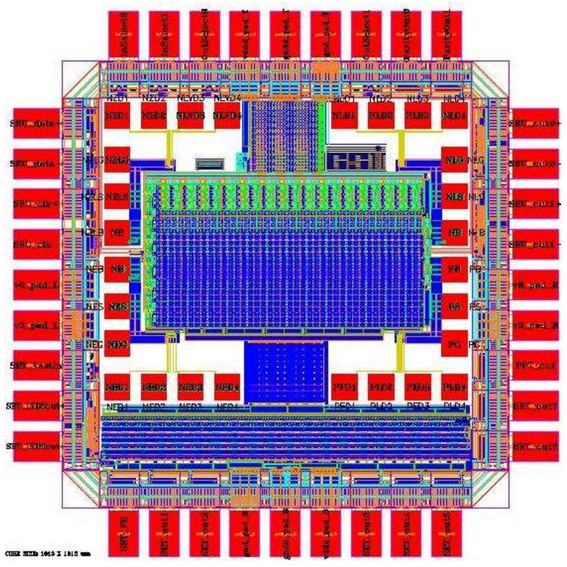

Fig. 1.: Layout of the GRISU test ASIC.

3 Single Event Effect Studies

Single Event Effect is the main generic term for effects in semiconductor devices triggered by the impact of ionising particles. Within the SEE there are more detailed types of effects. Of great interest for the future FAIR experiments are the so-called Single Event Transient (SET) and Single Event Upset (SEU) and effects.

3.1 Single Event Transient Test Structure

The minimal LET for a SEE failure at a given node depends on the load respectively the capacitance of this node. For measuring the critical charge at which a SET signal is generated, seven different inverter chains, different in node capacitance and transistor size, are implemented in the *GRISU* test chip. From analogue simulations the theoretical critical charge is well known for each of these structures. According to

$$\mathrm{LET}_{\mathrm{crit}} = \frac{Q_{\mathrm{crit}} \cdot 3.6\,\mathrm{eV}}{e \cdot \rho_{\mathrm{Si}} \cdot d} \qquad (1)$$

and an assumption for the sensitive depth d of the charge collection the critical linear energy transfer $\mathrm{LET}_{\mathrm{crit}}$ can be calculated. The design parameter of the used transistors are depict in Table 1 as well as the simulated critical charge and a realistic range for the critical linear energy transfer.

No.	W_{pmos} μm	W_{nmos} μm	C_{load} fF	Q_{crit} fC	$\mathrm{LET}_{\mathrm{crit,d=2\mu m}}$ MeV cm^2 mg^{-1}	$\mathrm{LET}_{\mathrm{crit,d=0.5\mu m}}$ MeV cm^2 mg^{-1}
1	0.48	0.24	1.24	32	1.54	6.17
2	0.96	0.48	2.39	58	2.80	11.19
3	1.92	0.96	4.68	114	5.50	21.99
4	2.88	1.44	6.99	172	8.29	33.17
5	5.76	2.88	13.87	344	16.59	66.35
6	11.52	5.76	27.62	674	32.50	129.99
7	23.04	11.52	55.91	1346	64.90	259.60

Table 1.: Design parameter, load capacitance, simulated critical charge and expected LET of the CMOS inverters

3.2 Single Event Upset Test Structure

For SEU testing two groups each consisting of four channels with up to 320 flip-flops cells were implemented on the test chip. Each of the eight channels vary either in layout modifications or in a different flip-flop architecture. The block diagram of one of these groups is shown in Fig. 2, the different flip-flop types and modifications cells are given in Table 2.

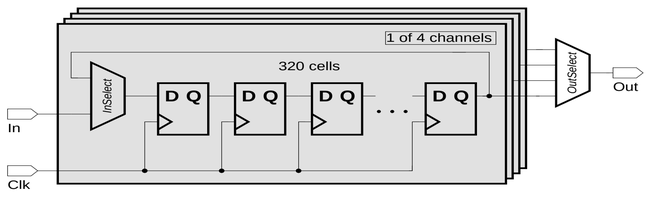

Fig. 2.: Block diagram of a flip-flop group for SEU testing.

Group 1	Group 2
Standard	Sense amplifier & DICE cell (based on [2, 3])
”sized” transistors	DICE cell based (based on [3])
internal buffers	”oversized” transistors
short routing	with long routing

Table 2.: Overview of the different flip-flop cells for SEU testing

4 Heavy Ion Irradiation Testing

Irradiating semiconductor devices with heavy ions is a good choice to measure SEE. All irradiation tests of the *GRISU* chip were performed at the GSI heavy ion linear accelerator UNILAC. The beam parameter at the transfer point to the experimental site is depicted in Table 3.

Beam parameters	
Available ions	all ions from Protons up to Uranium
Beam energy	11.4 MeV/AMU at exit window
Beam flux	$10^3 \ldots 10^{10}/(\mathrm{cm}^2 \cdot \mathrm{s})$
Beam size / location	50 mm in diameter, radiation in air
Bunch length / frequency	up to 5 ms / max. 50 Hz

Table 3.: Beam parameters for the low energy testing site

The necessary large LET range for a complete characterisation is obtained with different heavy ions. As the beam energy of the testing site is fixed, only the adjacent energy absorption in air after the exit window is changeable. An overview of the test setup position in beam and the resulting LET parameters for the available ions in 2008 and 2009 are shown in Fig. 3.

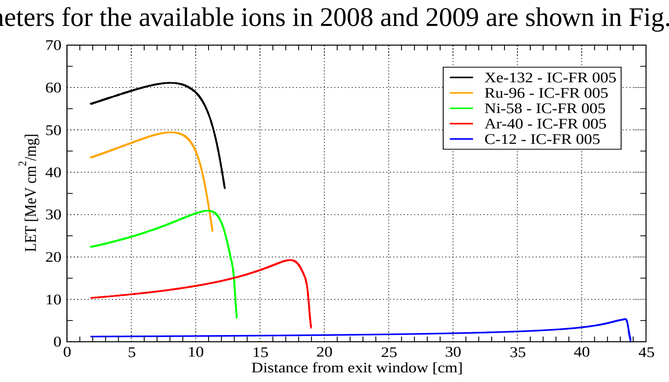

Fig. 3.: LET range for the available ions of the 2008/2009 testing.

The irradiation was done in bunches of heavy ions. The resulting SET events were counted by a FPGA instantaneously during irradiation. In contrast SEU events in the flip-flops were read out and analysed in the gap between two bunches. Together with the known number of heavy ion particles per bunch the cross section of each test structure is calculated.
As an example the overall SET cross section versus LET is shown in Fig. 4 for a minimum sized inverter (No. 1). The critical linear energy transfer as well as the maximum cross section are extracted with a Weibull fit and summarized in Table 4.

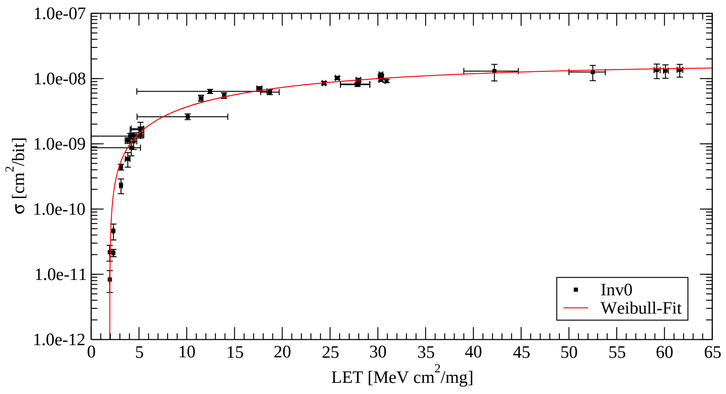

Fig. 4.: Weibull fit of the SET cross section of a minimum sized inverter.

Test structure No.	1	2	3	4	5	6	7
σ_{sat} [10^{-8} cm^2/bit]	1.35	1.48	1.69	1.78	1.77	0.89	0.08
$\mathrm{LET}_{\mathrm{crit}}$ [MeV cm^2 mg^{-1}]	1.939	1.945	2.021	1.953	1.900	1.899	1.898

Table 4.: Extracted Weibull fit parameter for different test structures

The comparison between the extracted $\mathrm{LET}_{\mathrm{crit}}$ and the simulated values from Table 1 shows a clear discrepancy. Up to now this behaviour is not completely understood.
Also there is rapid drop of the saturated cross section for test structures No. 6 and 7. To clarify and understand this decrease in sensitivity a so-called Single Heavy Ion Hit Microbeam test was performed (cf. section 5).
Furthermore the sensitivity against SEU of all types of flip-flops has been tested for different operation modes (e.g. static unclocked, static clocked and dynamic clocked mode). A comparison of the saturated cross section of the different flip-flop implementations is depict in Fig. 5.

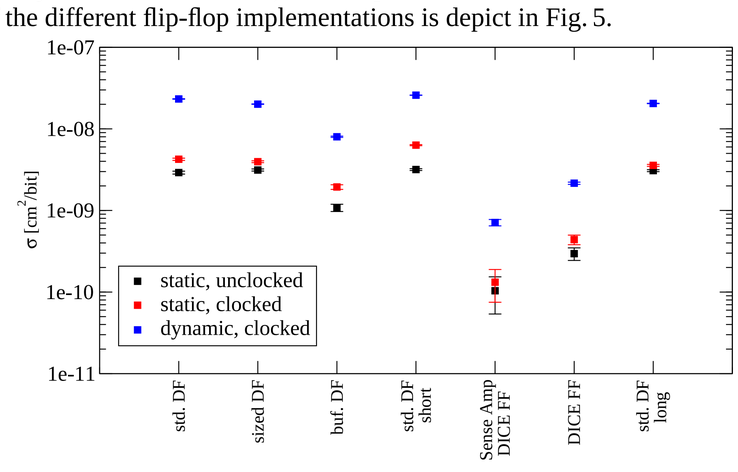

Fig. 5.: Saturated SEU cross section of all flip-flop test structures.

Both flip-flops with internal DICE structures respond more sensitive to SEU then expected from simulation. One possible explanation is a insufficient layout of the redundant transistors in these cells. A further microbeam test with a more accurate resolution might be helpful to understand this behaviour (cf. section 5 and Outlook).

5 Single Heavy Ion Hit Microbeam

The microbeam testing site is situated at the end of the GSI heavy ion linear accelerator. The ions entering the microbeam line through object slits are focused down to a focal spot of about 500 nm in diameter by means of magnetic quadrupole lenses. Deflecting magnets, situated in front of the focusing lenses, are used to move the beam spot in the focal plane. Available are all ions from carbon to uranium with energies up to 11.4 MeV/u.

A GRISU chip was irradiated with carbon at an energy of 4.8 MeV/u, corresponding to an LET of 2.25 MeV cm^2 mg^{-1}. The overall irradiating and scanning area was $80 \times 80\ \mu\mathrm{m}^2$.
As an example of these test results the layout overlay picture of the irradiated area and the observed SET events are shown in Fig. 6.

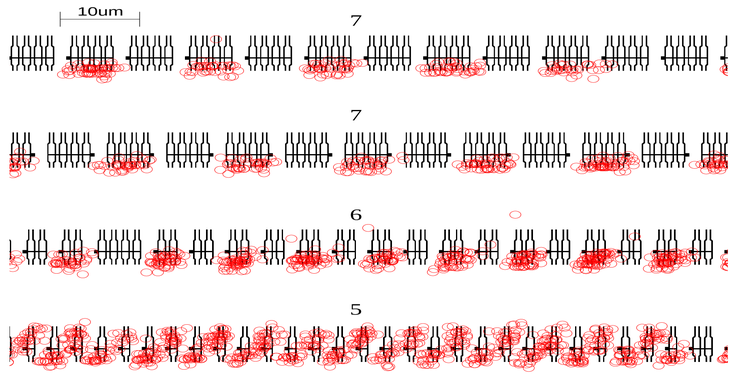

Fig. 6.: Overlay of inverter chain test structure layout and position of SET events. The radius of the circle is approx. 600 nm.

Each red circle represents a SET event. The centre refer to the measured origin of the microbeam DAQ system whereas the radius represents the 3σ position accuracy of 612 nm. For inverter chain No. 5 SET events were measured for NMOS transistors (lower layout part in each row) as well as for PMOS transistors (upper layout part). However for inverter chain No. 6 and 7 SET hits were only measured for NMOS transistors. The explanation for this is that the node capacitances of these PMOS transistors are larger compared to the smaller NMOS.
The first measurement show that the microbeam setup is a powerful tool for spartial resolving SEE investigations. However the resolution must be increased for closer investigations of the 180 nm process, especially for the study of the DICE structures.

6 Total Ionising Dose Studies

A TID test was performed at the X-ray irradiation facility of the Institute of Experimental Nuclear Physics (IEKP). In total 8 *GRISU* test chips have been irradiated up to 2.4 Mrad (SiO_2). The transient and output characteristics of all 16 discrete MOSFET transistors as well as threshold voltage and leakage currents were measured for different accumulated dose levels. Exemplarily the threshold voltage and leakage current of an NMOS transistor (W=0.24 µm, L=1.80 µm) is shown in Fig. 7. for different accumulated dose levels.

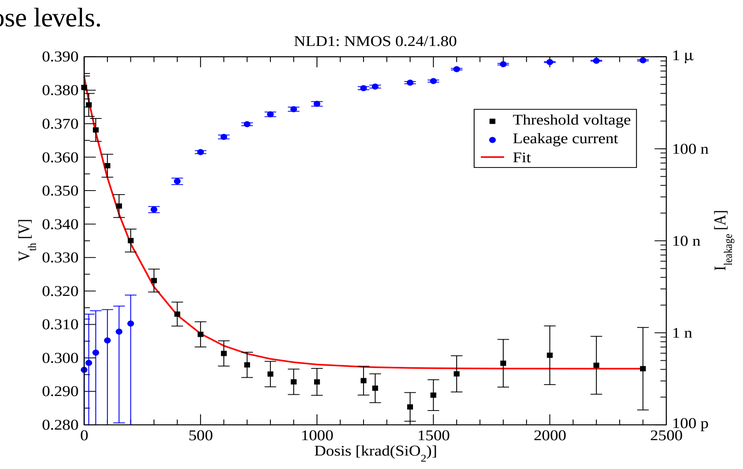

Fig. 7.: Threshold voltage and leakage current of a single transistor for different dose levels.

After total dose of 2.4 Mrad was exposed to an ASIC the measured leakage current for a single NMOS transistor increased by up to 3 orders of magnitude. In addition the long term annealing characteristics were monitored. Annealing of the chips was immediately observed after the end of irradiation. After four weeks, keeping the chips biased and at room temperature, the leakage current for all transistors had settled back to the initial value. Finally, all chips showed a very good annealing performance.

7 Summary and Outlook

A test ASIC for characterising the radiation hardness quality of the UMC 180 nm CMOS process was developed at the GSI ASIC design group. Furthermore a test site for heavy ion irradiation of complete ASIC chips as well as a heavy ion microbeam test site for single transistor irradiation have been set up at GSI. TID tests which have been done up to now have shown that this CMOS process is useful for future FAIR experiments. Especially the good TID annealing performance turned out to yield to no restrictions. SEE results have shown that maybe other techniques have to be used to decrease the sensibility to these events.
A second microbeam test will be performed with a more accurate resolution of approx. 100 nm for SEE position detection. Then it will be possible to scan the digital DICE flip-flop cell and map the origin of SEU and SET sensibility.

References

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