Radiation Studies on the UMC 180 nm CMOS Process

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Introduction

Radiation damages to electronic components are an important issue for future FAIR experiments. One of the preferred technology for ASIC developments at GSI is the 180 nm UMC CMOS process. In this regard the ASIC design group of the GSI Experiment Electronic department has been launched a research project in 2007, including the development of an ASIC called *GRISU*. The main goal is the characterisation of Single Event Effects as well as Total Ionising Dose effects on the 180 nm UMC process.

Single Event Effect Studies

Single Event Effect (SEE) is the main generic term for effects in semiconductor devices triggered by the impact of ionising particles. Within the SEE there are more detailed types of effects. Of great interest are the so-called Single Event Upset (SEU) and Single Event Transient (SET) effects.

A good choice to test these effects is the irradiation of the semiconductor devices with heavy ions. Therefore the *GRISU* test chip has been particular designed to monitor these effects during irradiation. For a complete characterisation it is also necessary to measure the impact of ionising particles at different Linear Energy Transfer (LET) levels.

The irradiation tests of the *GRISU* were performed at the GSI linear accelerator (UNILAC) in cave X6. The coverage of the large LET range was obtained with different heavy ions and energy absorption in air. An overview of the in 2008 available ions and the resulting energy and LET parameters are given in Table 1.

Heavy ion	Energy [MeV/AMU]	Energy [MeV]	LET [MeV cm^2 / mg]
C-12	0...10.4	0...125	1...5
Ar-40	0...8.8	0...352	7...19
Ni-58	0...7.7	0...447	15...32
Xe-132	0...7.2	0...950	30...60

Table 1: Energy and LET range for available heavy ions radiation tests in 2008.

Exemplarily the overall cross section test results versus LET is shown in Figure 1 for a minimum sized inverter. The critical Linear Energy Transfer (LET_{crit}) as well as the maximum cross section ratio are extracted from the test results for each test structures. Furthermore the sensitivity against SEU for different types of flip-flop and memory cells have been tested.

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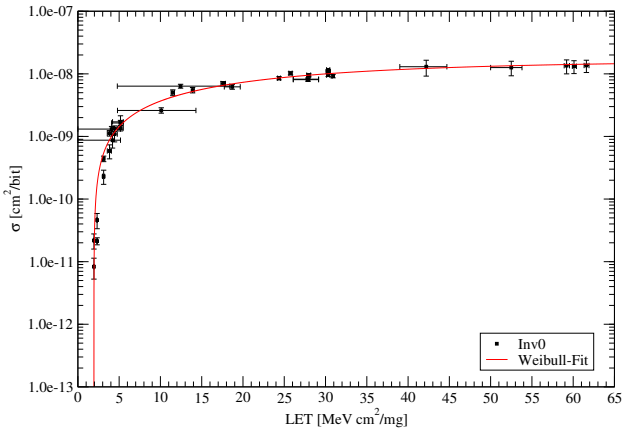

Figure 1: Weibull fit of the SET cross section of a minimum sized inverter.

Total Ionising Dose Studies

In July 2008 a Total Ionising Dose (TID) test was performed at the X-ray irradiation facility of the IEKP [1] / FZK [2]. In total 8 *GRISU* test chips have been irradiated. Table 2 summarises the different dose rates and accumulated doses.

The transient and output characteristics of discrete MOSFET transistors as well as threshold voltage and leakage currents were measured for different accumulated dose levels. Immediately after irradiation the annealing of the chips were measured. Finally, all chips showed a very good annealing performance. After four weeks leakage current has settled back to the initial value.

Number of chips	Dose rate [krad/h (SiO_2)]	Accumulated dose [krad (SiO_2)]
1	50	800
2	100	1000...1200
4	200	1600...2400
1	490	1500

Table 2: Summary of irradiated *GRISU* chips, dose rates and accumulated doses of the TID test.

References

[1] Institute of Experimental nuclear Physics (IEKP), University of Karlsruhe (TH) http://www-ekp.physik.uni-karlsruhe.de

[2] Forschungszentrum Karlsruhe (FZK) http://www.fzk.de