UMC 0.18µm radiation hardness studies

- Update -

Sven Löchner

13th CBM Collaboration Meeting

GSI Darmstadt

March 12th, 2009

Additional Talks & Documents

Reference to further talks:

- EE-Gruppenmeeting (7.7.2008)
  GRISU Statusreport
- CBM-XYTER Family Planning Workshop (5.12.2008)
  UMC 0.18µm radiation hardness studies
- IT/EE-Palaver (20.1.09)
  Untersuchung von Strahlungseffekten in anwendungs-spezifischen integrierten Schaltungen (ASIC)
  Strahlungseffekte

Link: http://wiki.gsi.de/cgi-bin/view/EE/GRISU

Reminder: GRISU project

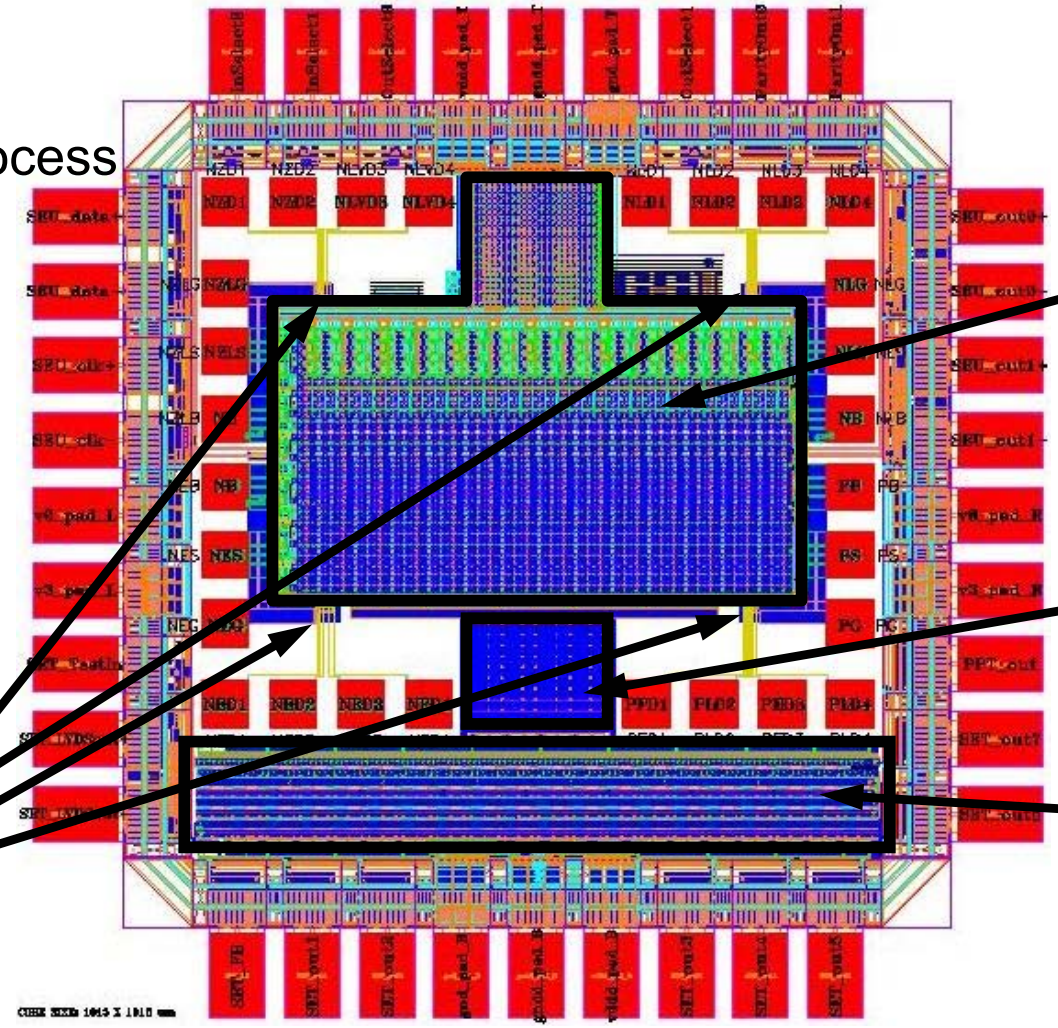
Project objectives:

- Characterisation of UMC 0.18µm CMOS process concerning the vulnerability against Single Event Effects (SEE), especially Single Event Upsets (SEU) and Single Event Transients (SET)
  - SEU cross section for different Flip-Flop designs and layouts
  - Characterisation of the critical charge Q_{crit} respectively the Linear Energy Transfer (LET_{crit})
  - SET sensitivity of the UMC 0.18µm process
- Single Transistor measurements
  - Comparison of transistor models by simulation
  - Total Ionising Dose (TID)
    Characterisation of the UMC 0.18µm process under irradiation, especially leakage currents, threshold shifts, annealing, ...

GRISU test ASIC

GRISU chip

- UMC 0.18µm process
- 1.5 x 1.5 mm²
- 64 pads
  - 28 core pads
  - 36 pads



Test structures for TID measurements

Test structures for SEU measurements

Ring oscillator for TID / SEU measurements

Test structures for SET measurements, Q_{crit}

SEE Building Blocks

3 different building blocks for SEE characterisation:

- Test structures for SEU measurements
  - 8 different types of flip-flops implemented, e.g. oversized flip-flops, flop-flops with Dual Interlock Cell (DICE) architecture, ...
- Test structures for SET and Q_{crit} measurements
  - Different inverter chains
    => $Q_{crit,sim}$ from 20 ... 1000fC
- 2 ring oscillator test structure

Low Energy testing site

- Installation of a test facility for ASIC irradiation with heavy ions at X6 cave at GSI (in cooperation with bio physics group)
- Beam monitoring via ionisation chamber
- Dosimetry setup available
- Irradiation of DUT in air
- Easy access

X6 cave at GSI

Disadvantages of setup:

- Only one ion source during beam time
- “Fixed” LET range for ion source

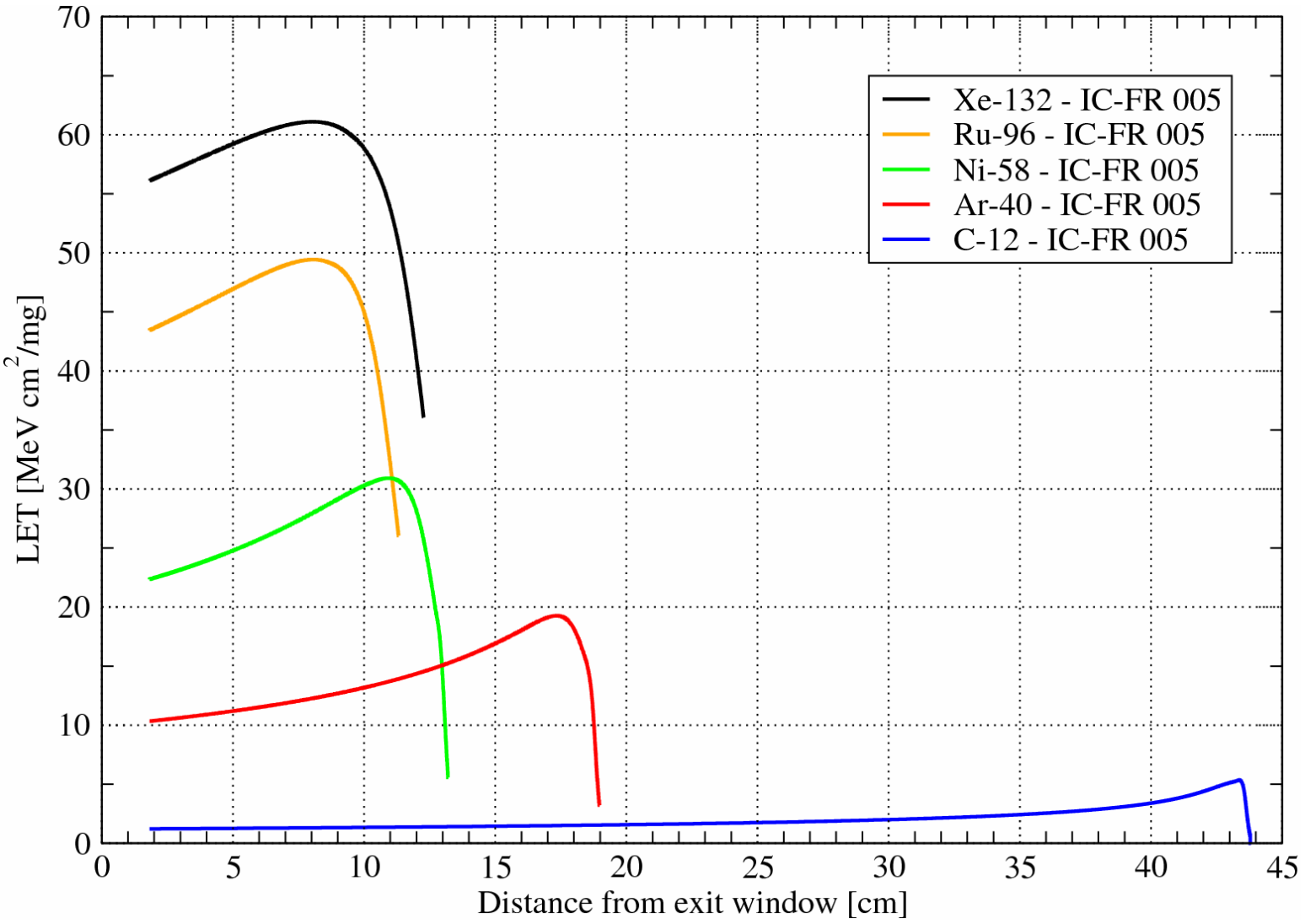
SEE Tests at GSI

SEE test with heavy ions at GSI:

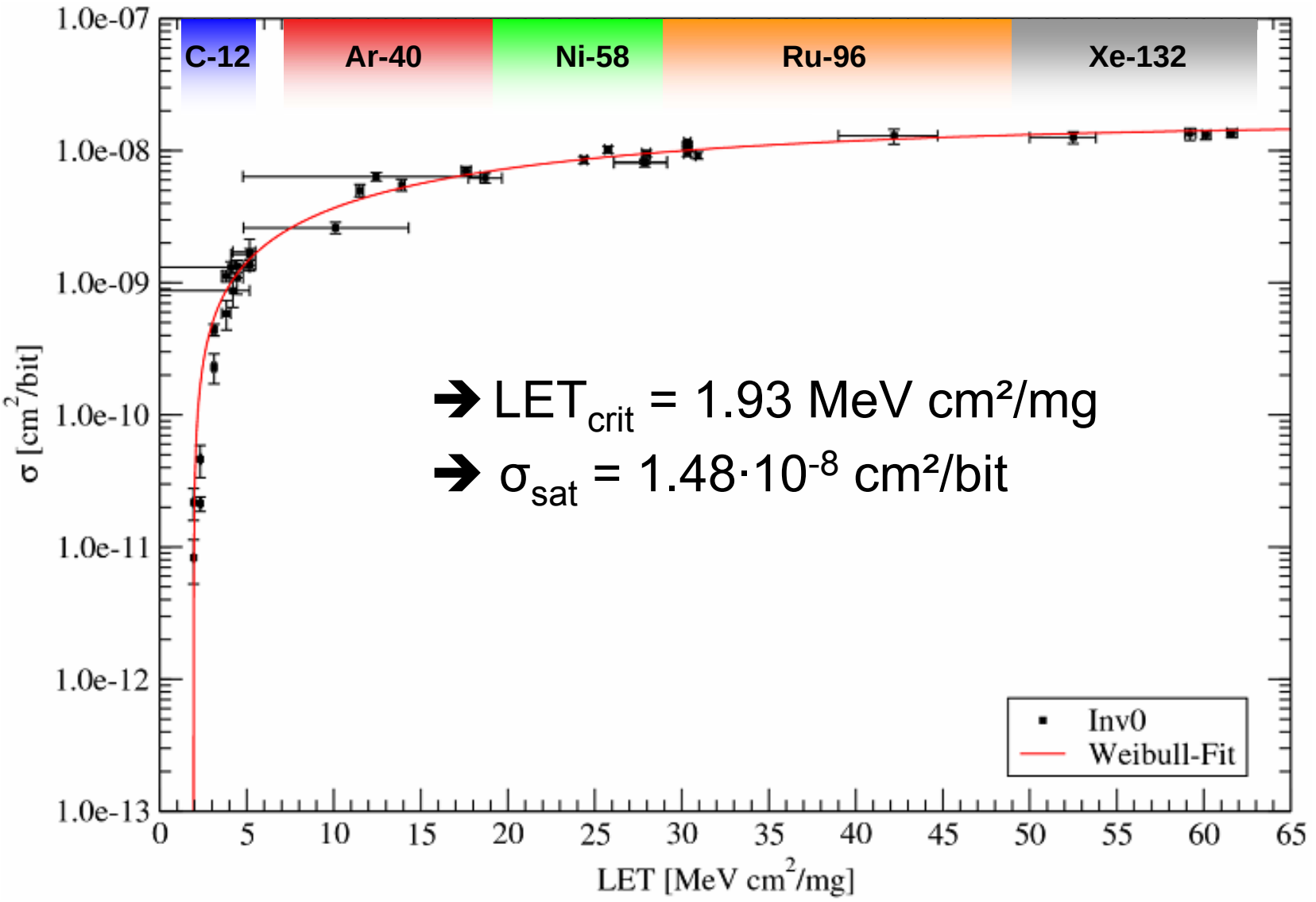
- X6 experimental site
- 11.4 MeV/u
- 7 irradiation tests so far
  - C-12 (3x)
  - Ar-40
  - Ni-58
  - Ru-96
  - Xe-132
- LET in the range of 1...62 MeV·cm²/mg (SiO_2)
  ➔ Q = 8..1300 fC

LET testing range

Overview of the LET testing range for the applied heavy ions test



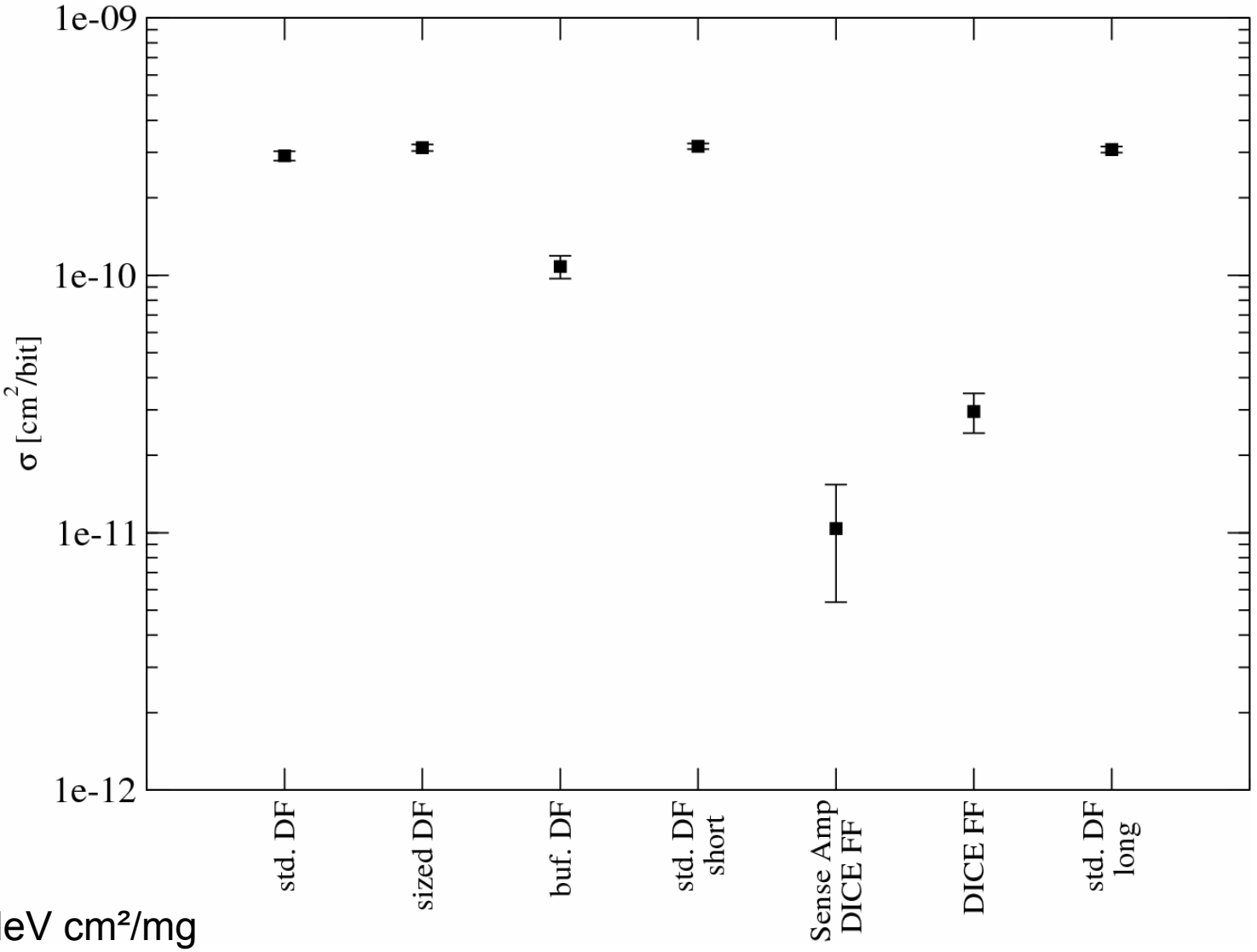
Cross-section (Weibull-Fit)



➔ LET_{crit} = 1.93 MeV cm²/mg

➔ $\sigma_{sat} = 1.48 \cdot 10^{-8}$ cm²/bit

Cross-section (DF)



LET = 4 MeV cm²/mg

Dual Interlock Cell (DICE)

DICE (Dual Interlock Cell) memory technologies are (more or less) immune against SEU flips.

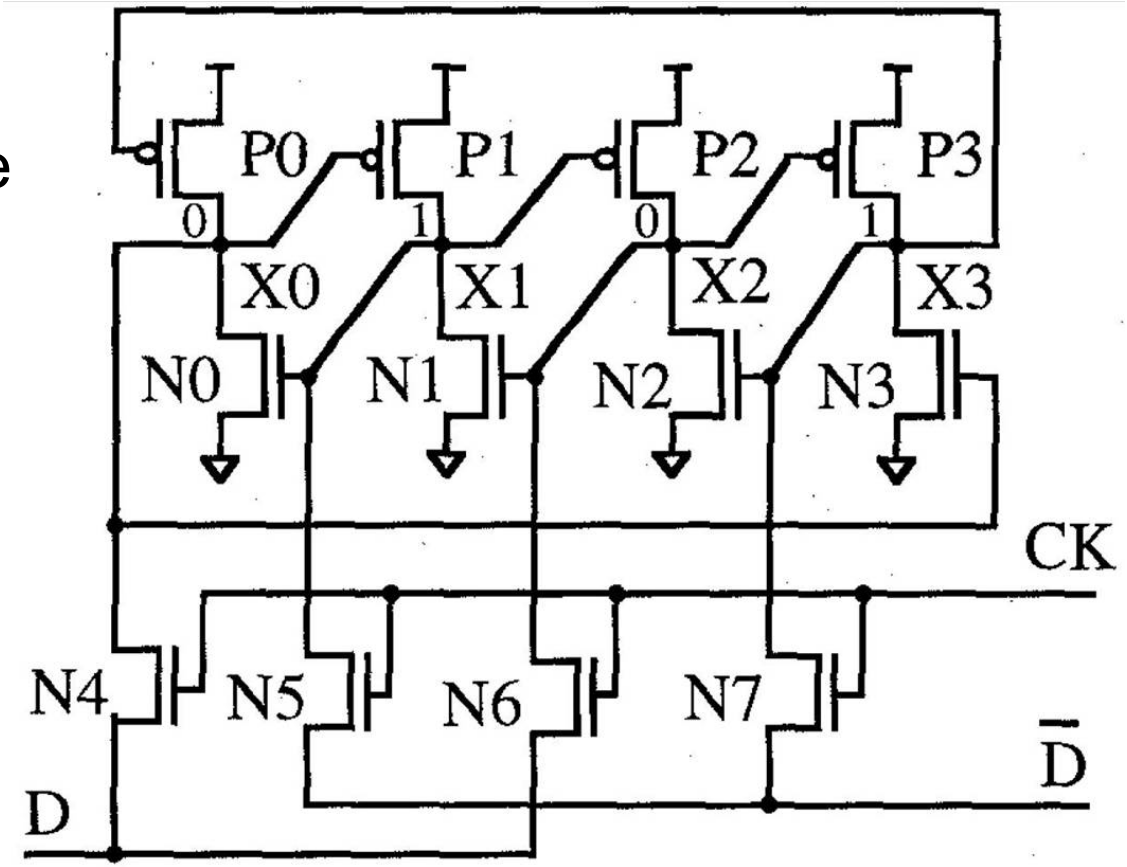
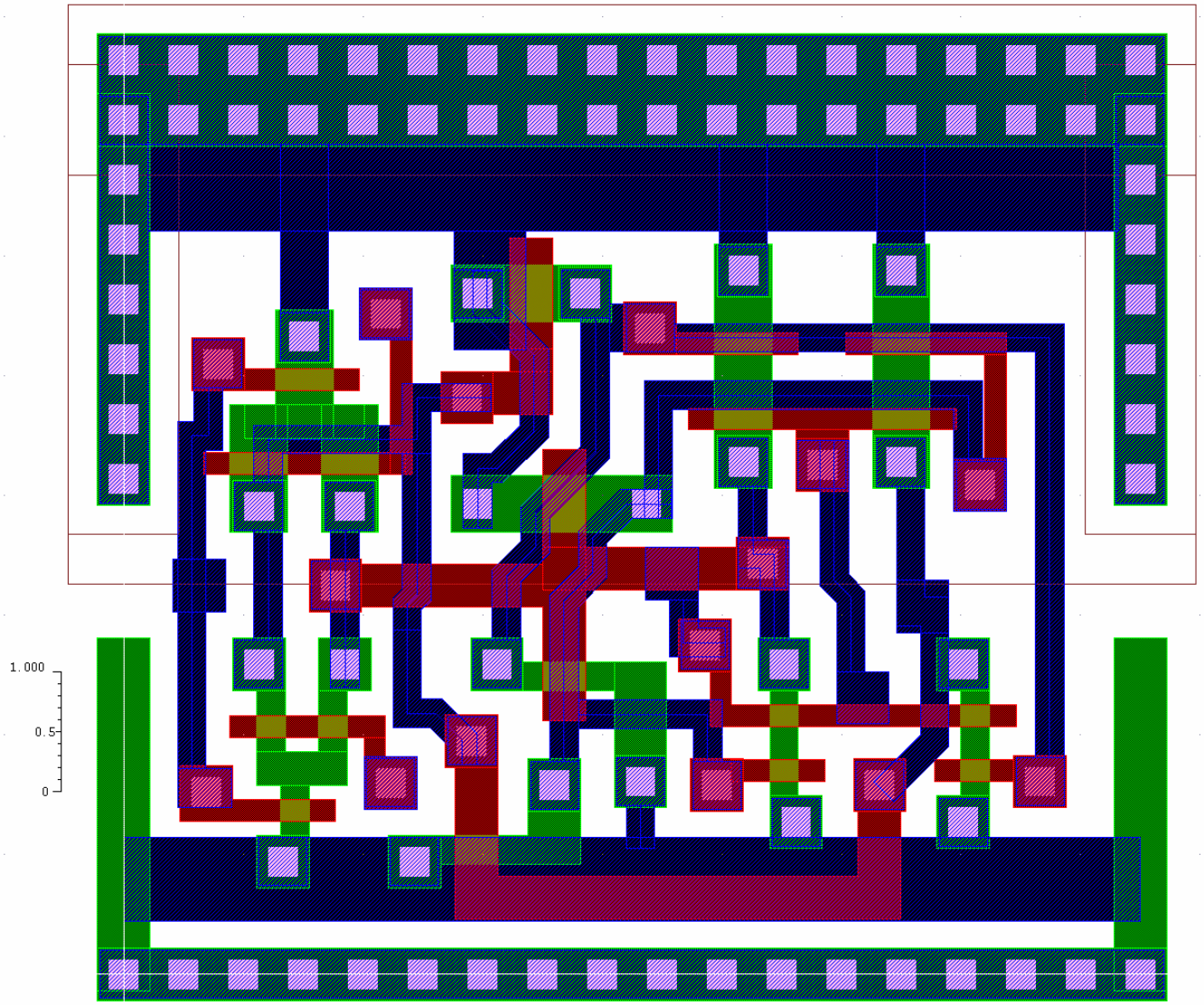


Fig. 4. The DICE Memory Cell

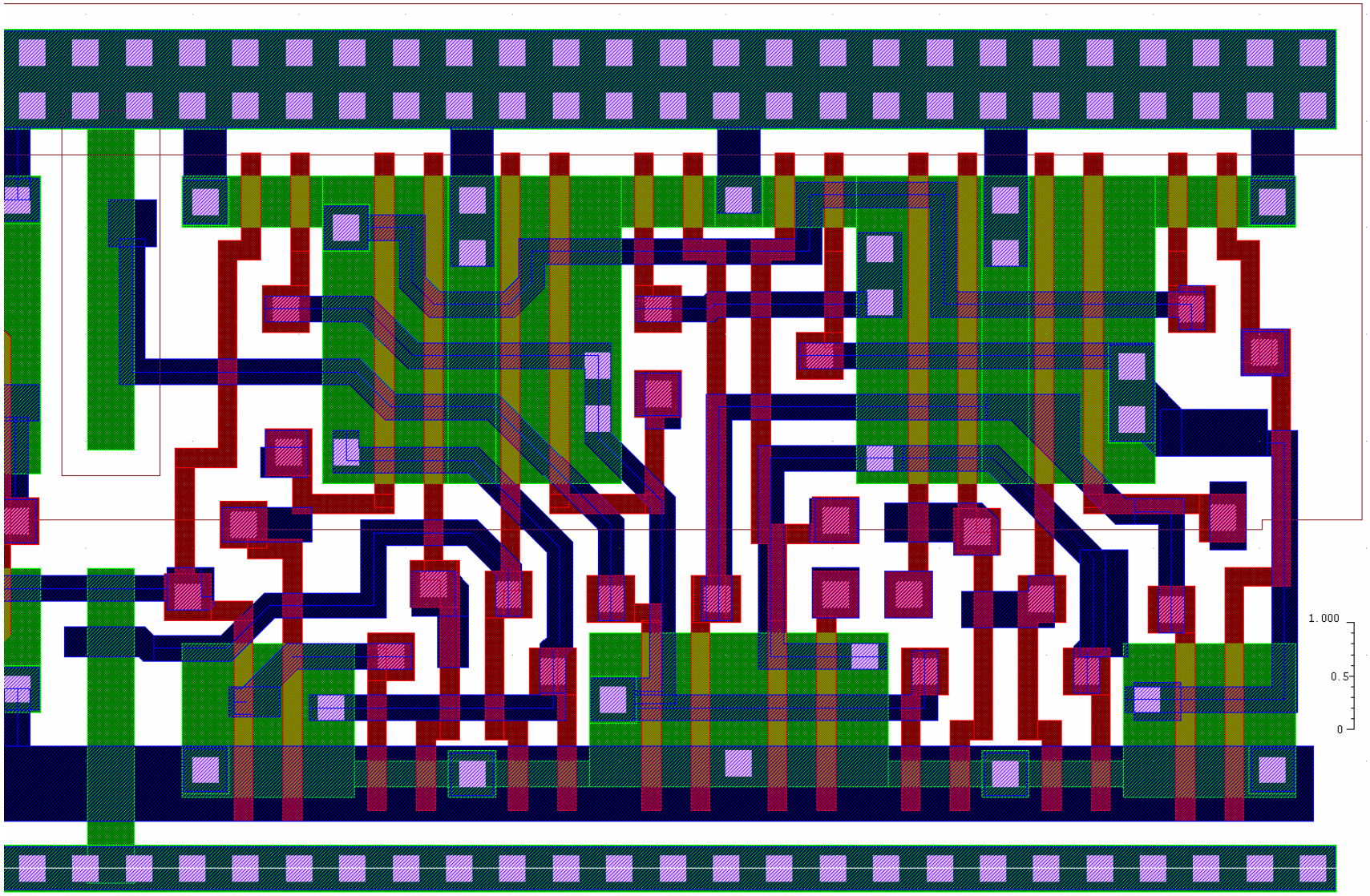
Reference:

T. Calin, M. Nicolaidis, R. Velazco
Upset Hardened Memory Design for Submicron CMOS Technology
IEEE Transactions on Nuclear Science, Vol. 43, No. 6, December 1996

Layout DICE Latch



Layout Sense Amp. DICE FF



SEE Summary

- Setup of a heavy ion test environment for ASIC irradiation
  - defined LET value within a range from 1...62 MeV·cm²/mg (SiO_2)
- Measurement of SEE cross-section for different design cells
- No SET observed on clock lines
  - ➔ capacitance of clock lines high

Not really understood:

- Higher sensitivity of DICE cells than expected
  - ➔ Heavy ion micro beam scan setup

Maybe on a next chip iteration:

- Triple redundant testing (SEU / SET improvement)

GRISU 2 – test structures

- Access to single transistors via core pads
  - small pad geometry
  - close to neighbour test pads

- 16 test structures
  - NMOS
  - PMOS
  - zero-Vt and low-Vt
  - special transistor layouts (e.g. enclosed, finger)

- Automatic measurement of transistor characteristics
  - Output characteristic (U_{ds} – I_{ds})
  - Transfer characteristic (U_{gs} – I_{ds})

Total Ionizing Dose (TID) tests

- TID testing with X-rays
  - Irradiation facility at Institute for Experimental Nuclear Physics, University of Karlsruhe
  - 60keV X-ray
  - 100 ... 600krad/h
- 9 GRISU chips tested
  - Total dose between 800krad and 2500krad(SiO_2)
  - Operating dose rate between 200krad/h and 580krad/h
  - Two radiation test modes
    - single transistor test structure measurements
      leakage current, threshold shift, characteristics
    - complete chip measurements
      transition times, total power consumption

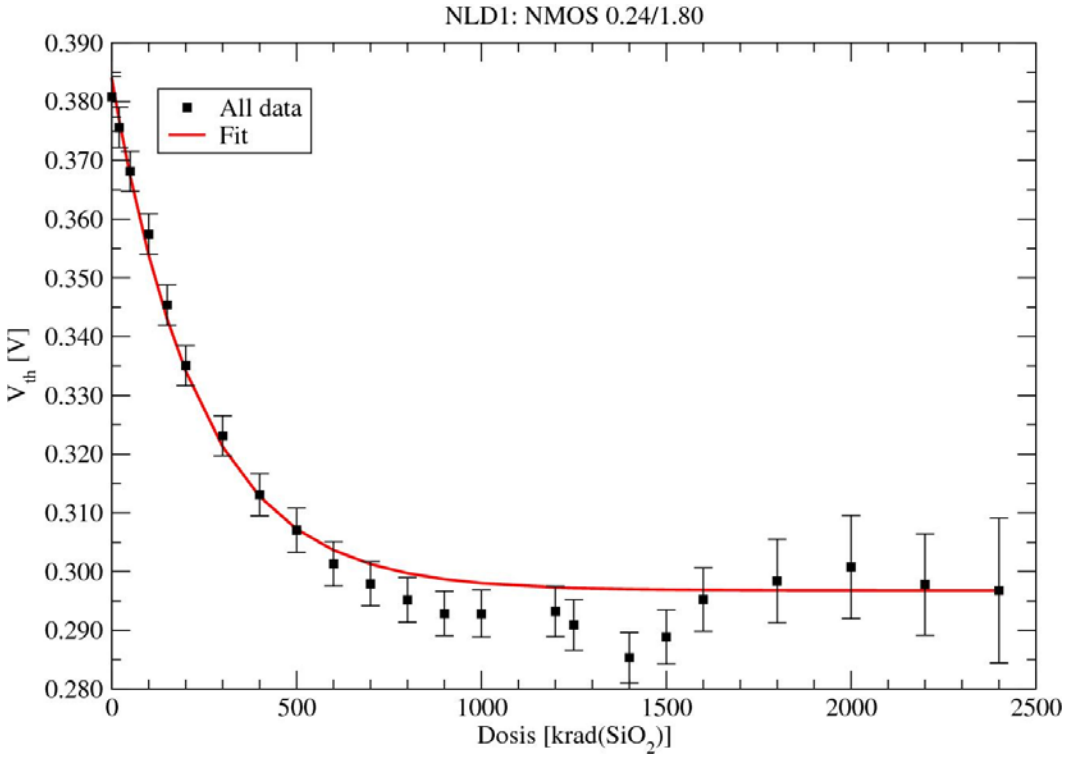
TID tests – complete chip

- Power consumption (Pads)
  - Increase of power consumption by factor of 100 after 1.5Mrad
    - ➔ Leakage current of ESD protection diodes
  - Good annealing at room temperature
    - ➔ back to pre-radiated value after 6 weeks
- Power consumption (Core)
  - Increase by factor of 2 after 1.5 Mrad
  - Also good annealing at room temperature
    - ➔ back to pre-radiated value after 6 weeks
- Transition times of minimum size inverter (ring oscillator)
  - Gets slightly faster up to 250krad
  - Beyond 250krad noticeable slower
    - ➔ unbalanced NMOS / PMOS ration of inverter
  - Good annealing at room temperature

TID tests – single transistors

Measurements of the transistor characteristics and calculation of the threshold voltages for different dose levels

- In total 6 chips are irradiated
- Total dose up to 2.5Mrad
- Dose rate between 200krad/h and 580krad/h



TID tests – single transistors

- Threshold voltage (Vth)
  - Almost no further threshold shift after 1Mrad observed
  - Larger NMOS Vth shift for smaller *W*
  - Constant Vth for enclosed transistors (as expected)
  - More or less no Vth shift for PMOS transistors
- Leakage current
  - No significant increase up to 200krad
  - Scales with gate length *L* (NMOS)
  - Zero-Vt: already high leakage current for pre-radiated transistor (≈ 0.5µA)
  - No increase in leakage for enclosed and PMOS transistors
- Annealing
  - Recovery of Vth in the order of 20-40% after 6 weeks
  - Leakage more or less back to pre-radiated values after 6 weeks

TID summary

- UMC process shows good annealing at room temperature (at least at high dose rates)
- Simulation models slightly differs from measured characteristics (especially between small and large Ugs)

Still to be done

- Second irradiation campaign with low dose rates
- Long term test with a gamma source

Thank you