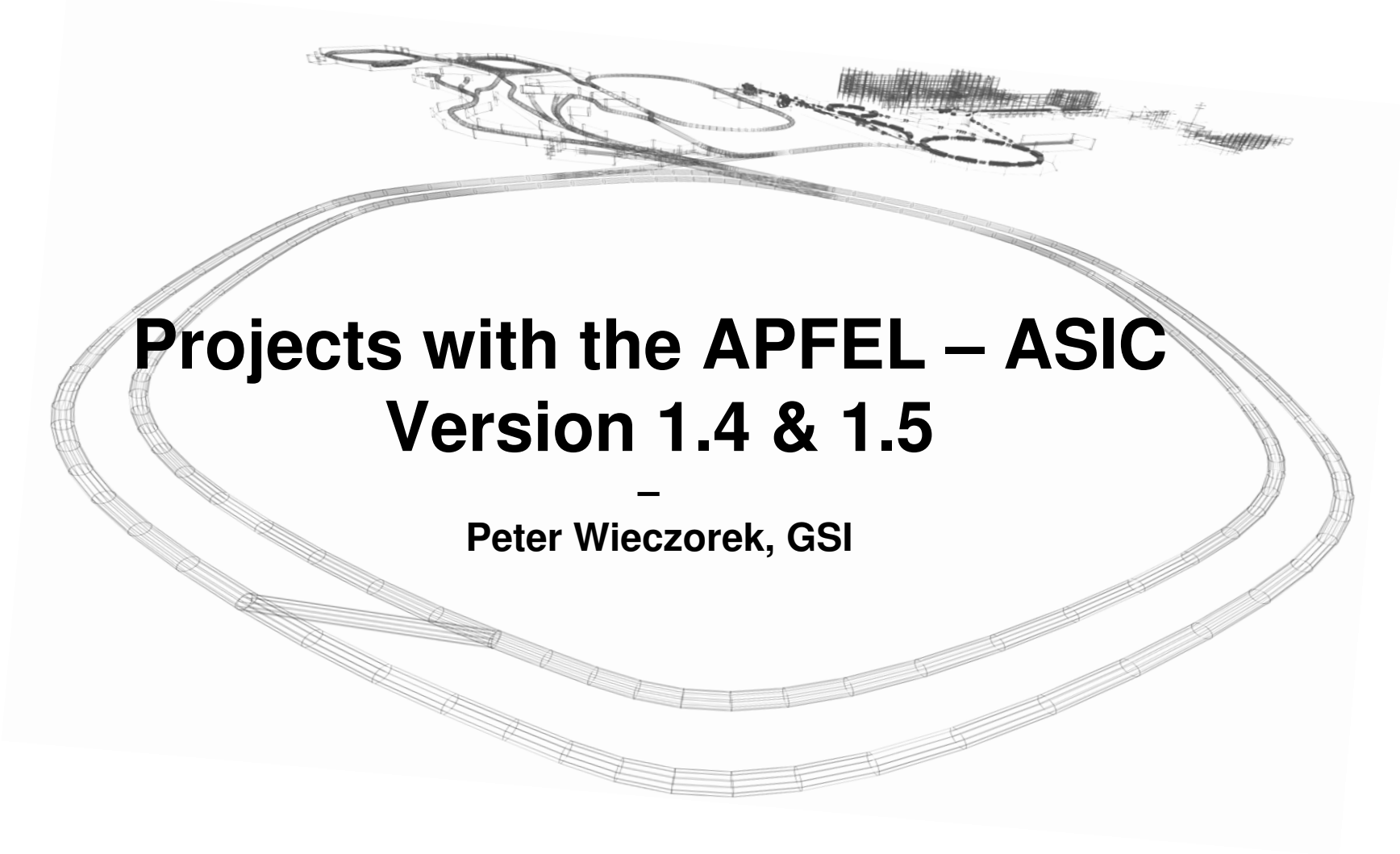

Projects with the APFEL – ASIC Version 1.4 & 1.5

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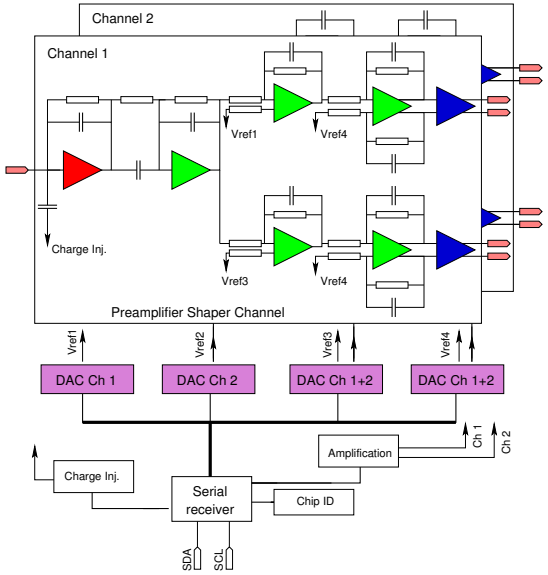
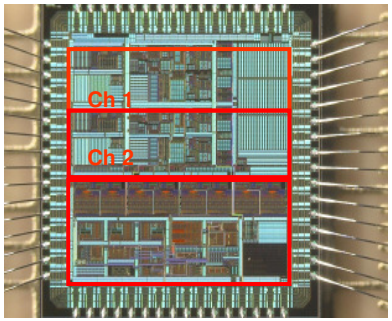
Peter Wieczorek, GSI

APFEL – ASIC



APFEL ASIC 1.4



APFEL ASIC 1.4/1.5 overview:

Analog Readout:

- Each readout channel consist of
  - charge sensitive preamplifier
  - third order shaper stage
  - differential output driver
- Two outputs per channel with different amplification to cover the dynamic range
- Two equivalent channels per chip

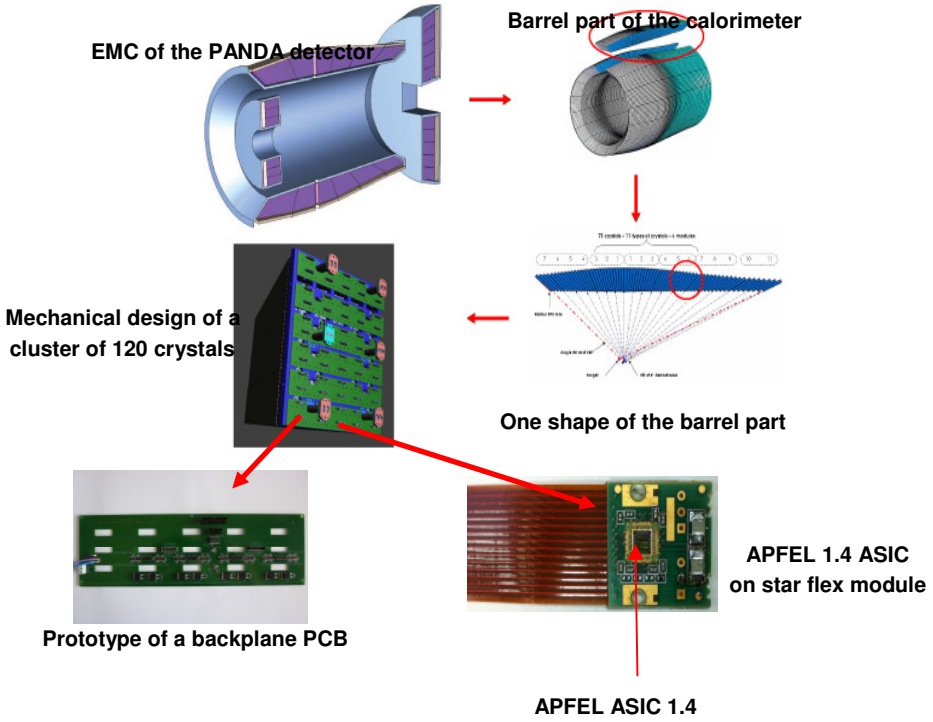
Digital Part:

- Three wire serial interface for:
  - Trigger of auto calibration
  - Read and write of the DAC settings
  - Charge injection for test pulse generation
  - Chip ID for single chip bus communication

	Required at T = - 25 ° C	Results at T = - 25 ° C	Unit
Integration time:	250	252 ± 3	ns
Noise:	4500	4125 ± 67	e^-
Max. input charge:	7	8	pC
Dynamic range:	>10000	>10000	1
Event rate:	350	350	kHz
Power consumption:	< 60	58 ± 1	mW

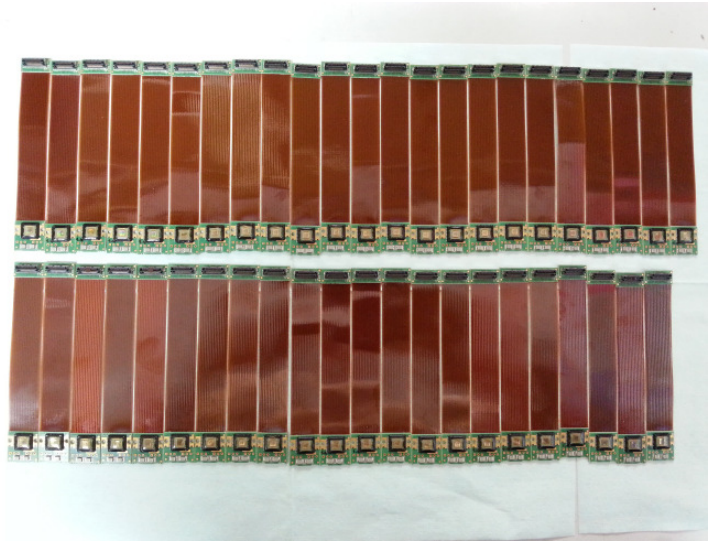
1. PANDA Barrel: Proto 120

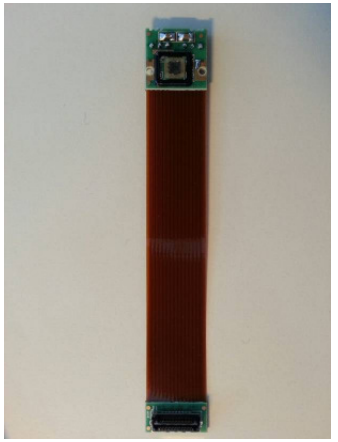
- **Barrel prototype:**
  - Operation temperature of the setup: -25 °C
  - 120 crystals with 2 APDs
  - One ASIC (2 channels) per crystal
  - Start version: 40 crystals
  - Differential line driver
  - Differential ADC readout (STRUCK ADCs)
  - Mounting of the setup at Giessen
  - Beam time (End 2013) in Mainz



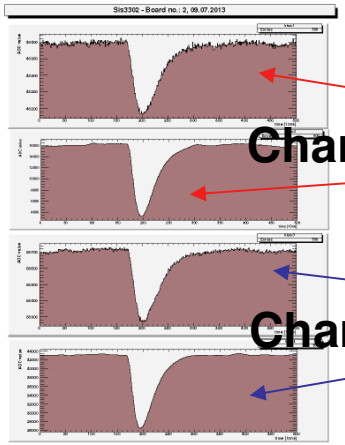
Status of Proto 120

- **Status of Proto 120:**
  - 45 flex modules are ready
    - Assembled, die and wire bonded and protected with glop-top
  - Connector to APDs are missing
    - Coming from Giessen
  - First test at GSI at RT
    - With 2 APDs on one crystal
    - and FEBEX readout
  - Second test in Giessen at RT
    - With 2 APDs on one crystal
    - STRUCK ADC readout
  - Mechanical changes are done
  - APD characterisation missing
  - Mounting: September 2013

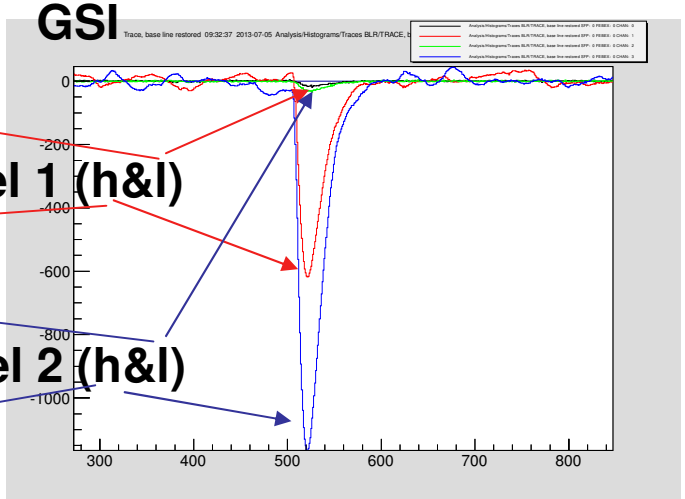




GI



GSI



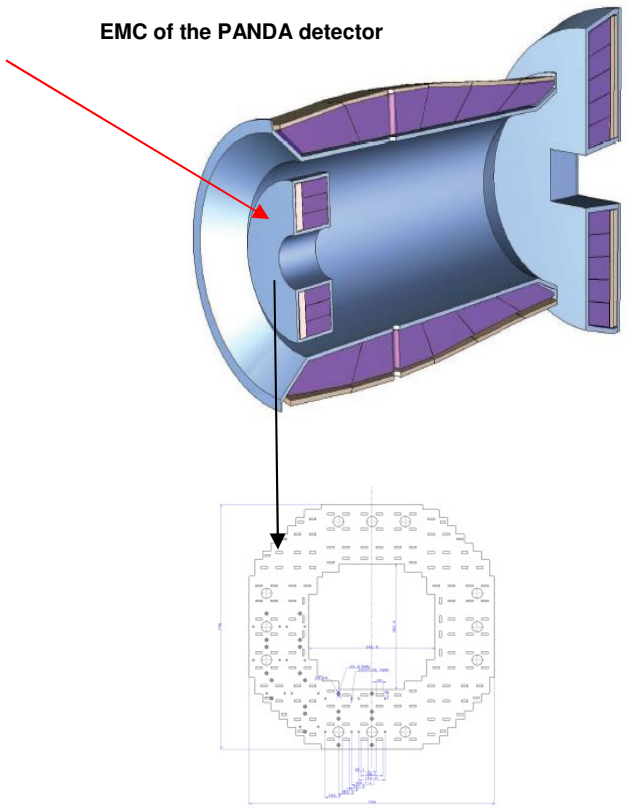
Channel 1 (h&l)

Channel 2 (h&l)

2. PANDA B-E-Cap: Proto 18

- **Readout for PANDA Backward – End – Cap (B-E-Cap) consisting of 524 single crystals**

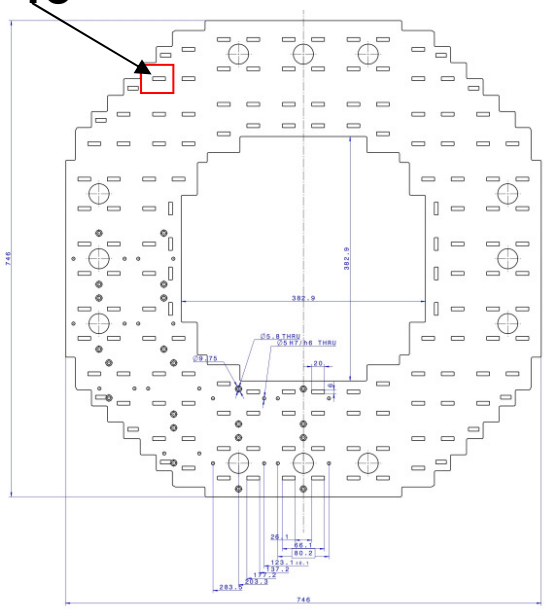
- **Design based on the Proto 120 but with other geometry**
  - **New flex ASIC PCB**
  - **New backplane PCB**
  - **But: Digitalization with FEBEX**
  - **Data readout & analysis: MBS and Go4**



Status of Proto 18

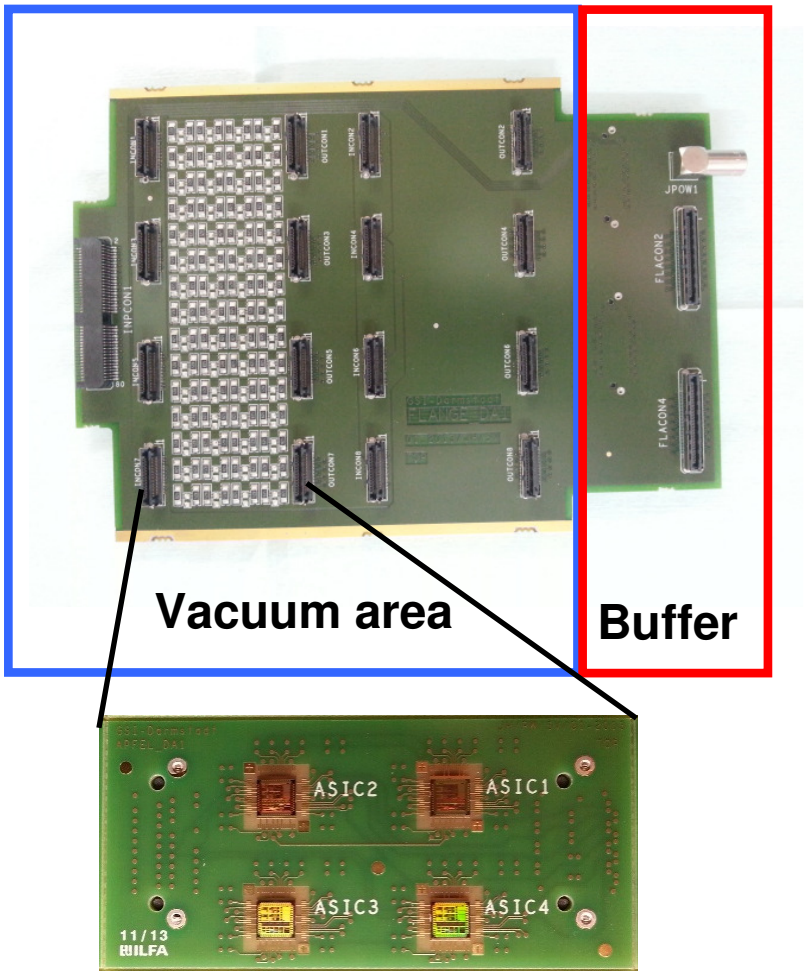
- **Status of Proto 18:**
  - **DAQ (MBS, FEBEX, …) is ordered**
  - **PCB design**
    - **New flex PCB has to be designed – maybe!**
    - **New backplane PCB is required and the schematic is ready**
    - **The layout of the backplane PCB is difficult because of 18 different geometries**
  - **APFEL ASICs**
    - **Additional 75 APFEL 1.5 ASICs will be ordered for several tests**

Proto 18



3. SHIP: Si – Strip Detector Readout

- **Design of several PCBs**
  - Motherboard PCBs
  - Plug – in ASIC PCBs
  - Buffer PCBs (@ work)
- **Overview**
  - FEE placed close to the detector (cooled (-10 °C and in vacuum)
  - Readout of 64 x 4 strips
  - Totally: 512 differential outputs (h&l)
  - Outside the buffer will be placed to drive a 2m line to the ADC readout
  - Programming the ASICs with the FPGA on the FEBEX PCB



SHIP – Scheduling

- **Status:**
  - 8 backplane PCBs are assembled
  - 2 ASIC PCBs with 4 ASICs each are ready for detailed tests
    - Totally 34 of these 4 ASIC PCBs are required
    - Glop-Top will be used as protection
    - For cooling an aluminum or copper block will be used which has to be connected to the detector cooling pipe
  - Buffer design is ready (Layout is started)
  - First test of thermal conductivity are done by a summer student (Ryan Wilkinson)
  - Full test with a detector has to be done (will be done end of 2013)