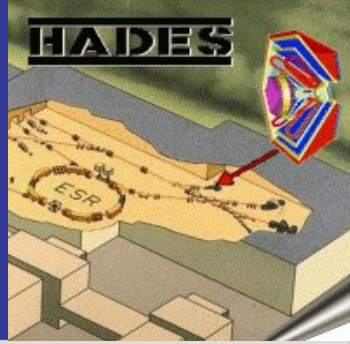

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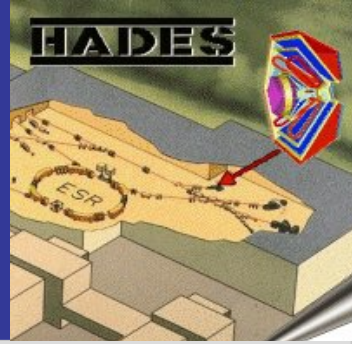
The new HADES Trigger Bus

Ingo Fröhlich

GSI – 17.7.2006

The HADES Trigger



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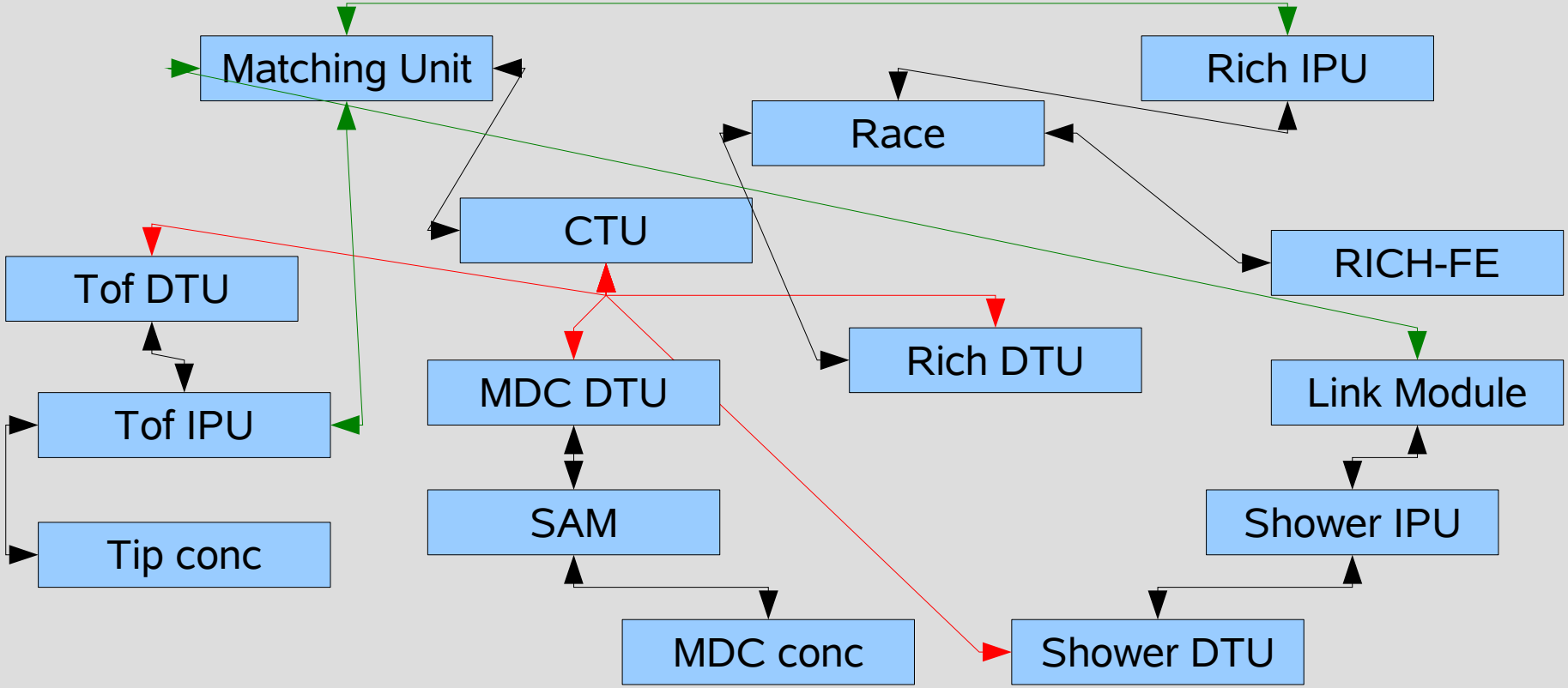
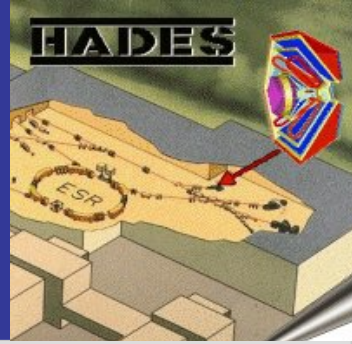


- All black arrows are stand-alone protocols
  - Trigger bus (red)
  - MU bus (green)

Trigger Bus: Simplified View



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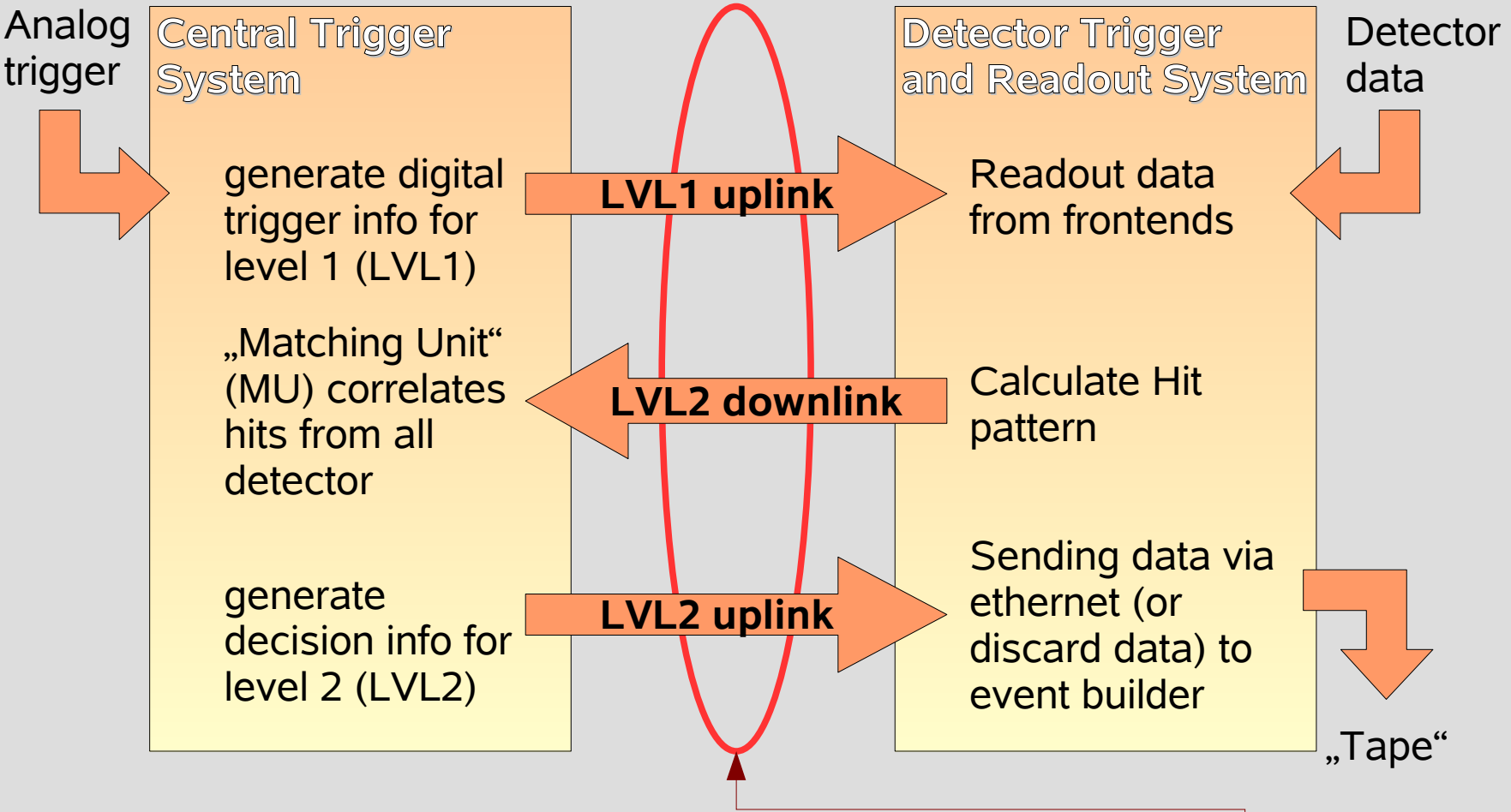
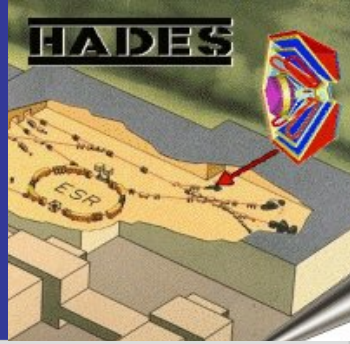


- Communication done via 3 flat cables

Problems



- Too many individual components
  - All with their own debug tools etc...
- Thinking in „units“ (Detector Trigger Unit, Central Trigger Unit, Matching Unit, Image Processing Unit)
  - Very often „project“ of a PhD-Theses, optimized for algorithms, not for communication
- Too many individual links/busses (IPU-Link, Trigger Bus, TIP-concentrator, CTU-MU, DTU-Backplane, IPC-Link, RACE-PRC, etc...)
- Links have no debug feedback
- Need to login on several CPUs -> Already now a mess

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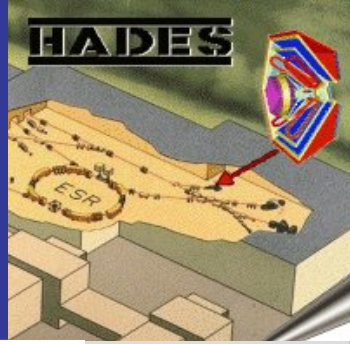
The New Concept (for the TRB Project)



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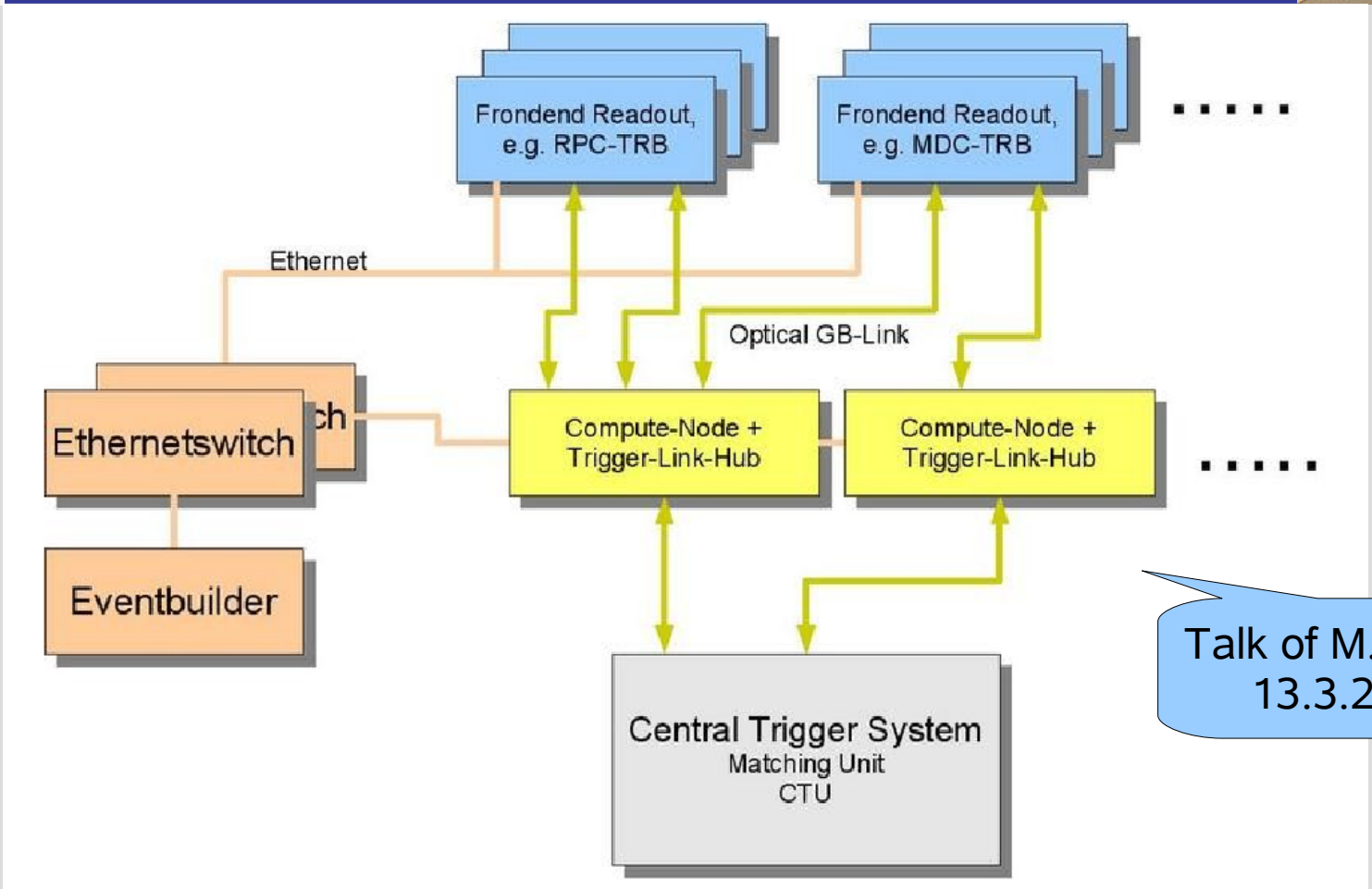
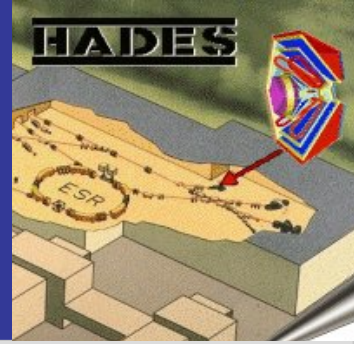


- Merge at least MU- and trigger bus
- Use point-to-point connections (optical links)

New HADES Trigger Network



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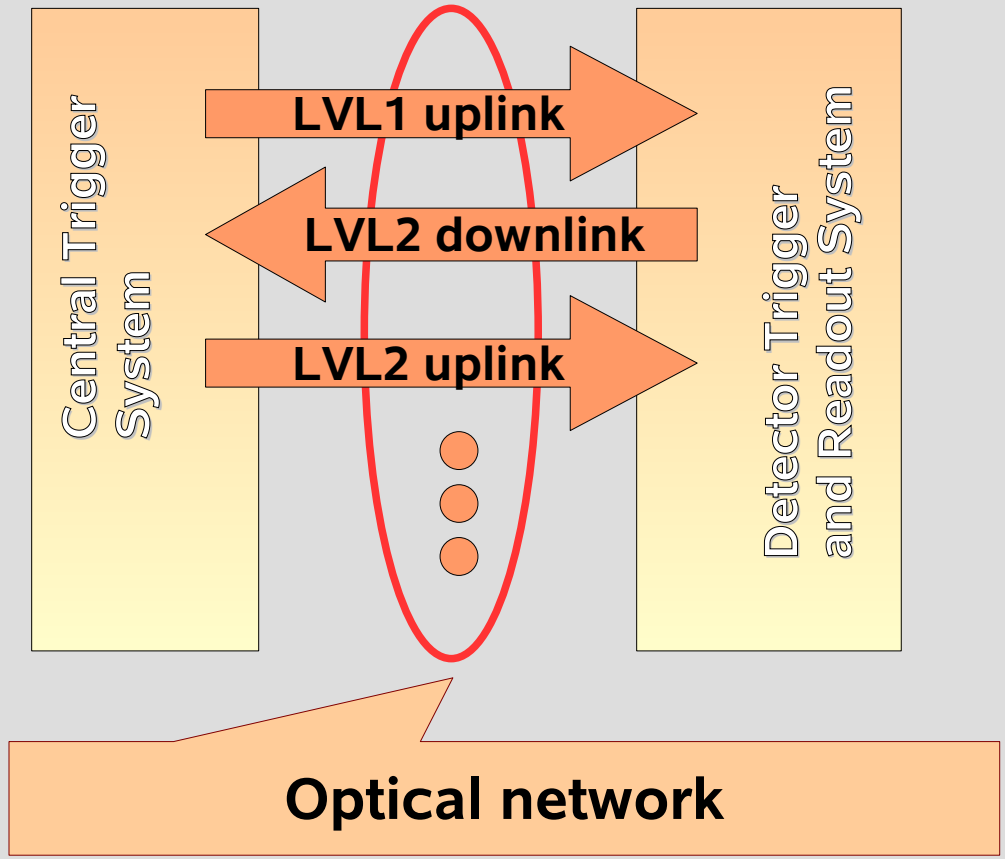
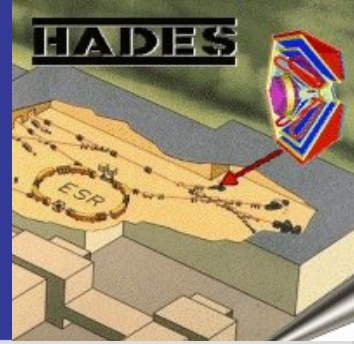
- Requirements
  - Latency*hub-levels adds to deadtime
    - Low-latency (150-250ns)
  - No high-level OSI-layers possible
    - No data loss on the network layer
    - Needs back-pressure
  - Trigger logic hidden in the network layer
  - Adaptable to *small* FPGAs and *any* medium bandwidth



New HADES Trigger Network



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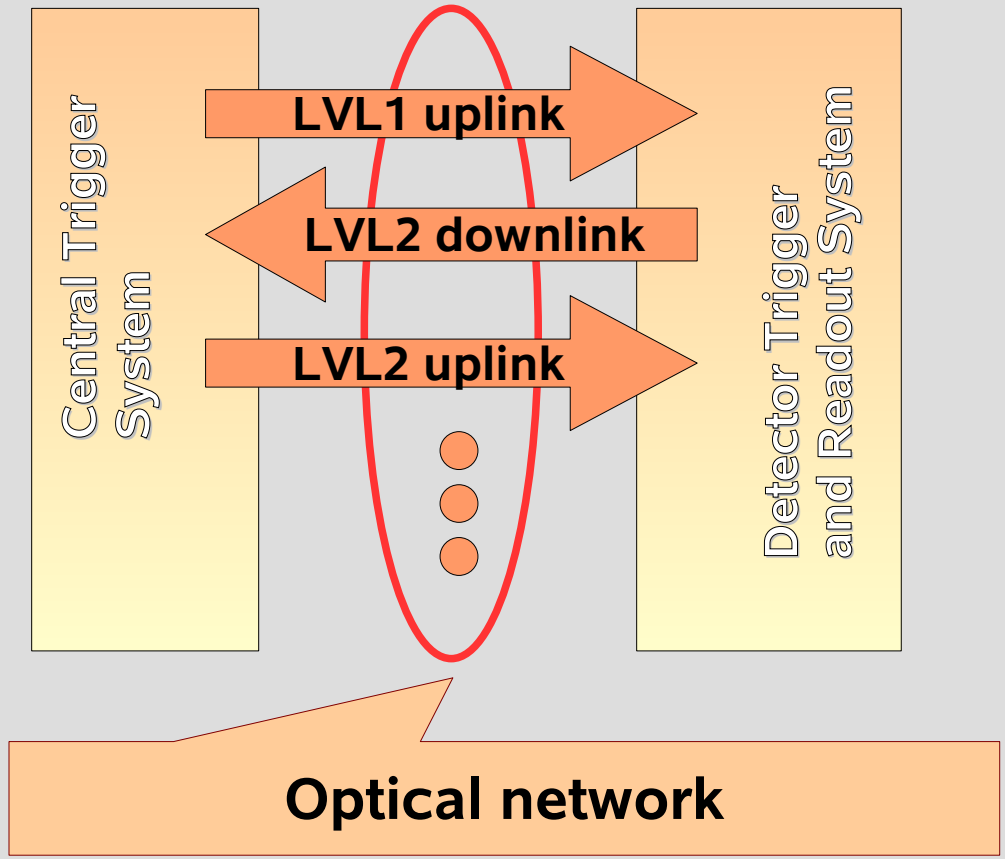
- 3 simple layers

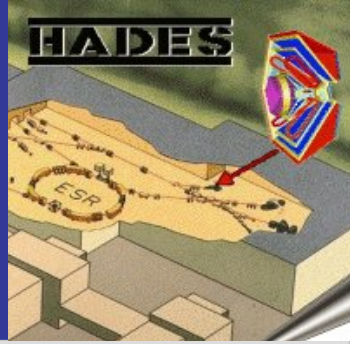
Data
Source/target address
Trigger tag & code
Slow control

Network
Locking & busy logic
Data integrity
Multiplexing

Medium
Optical, 8B/10B
LVDS-cable
Connector for TRB-AddOns



Virtual Channels



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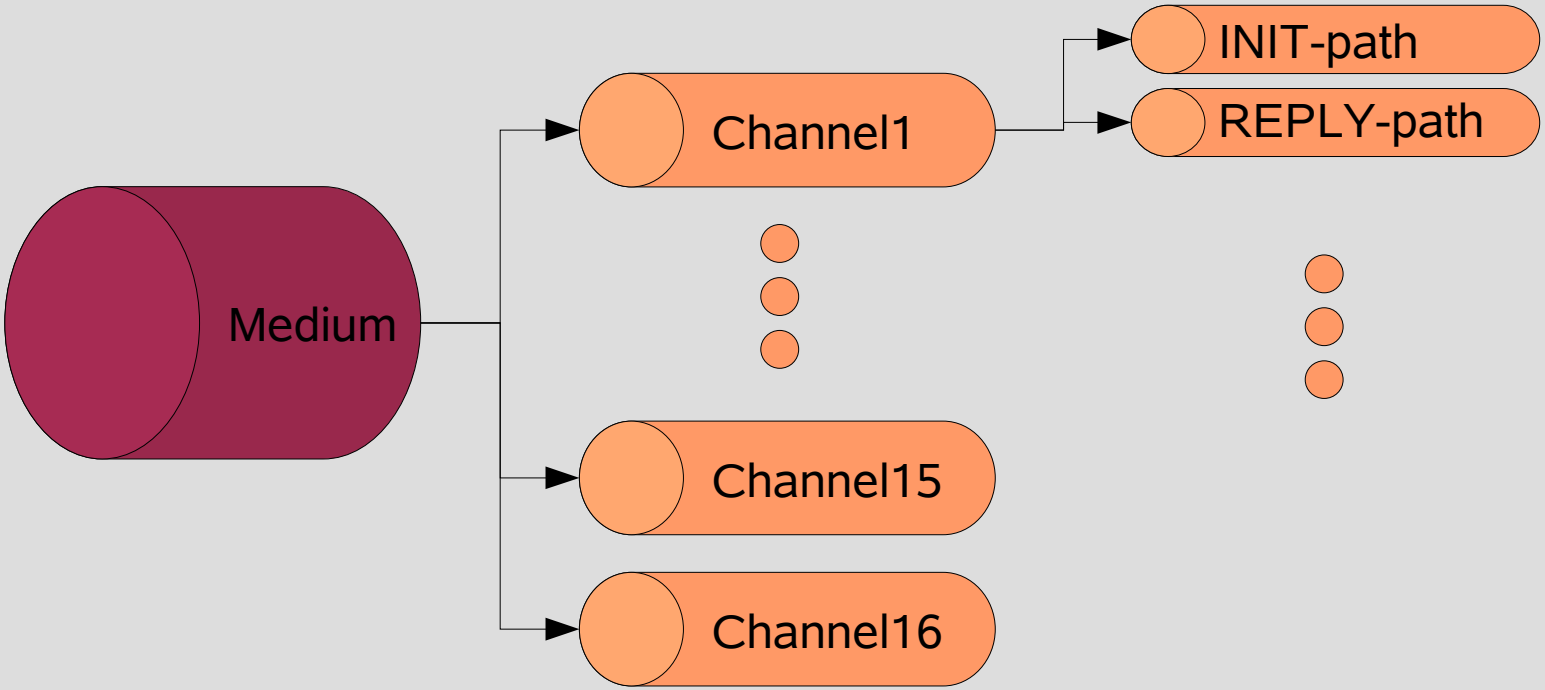
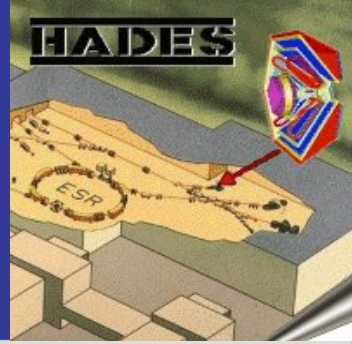
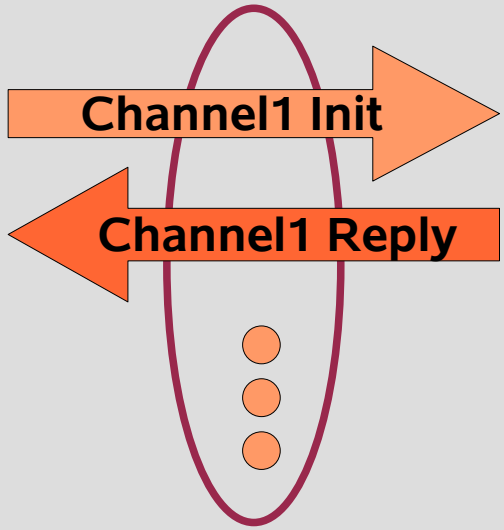


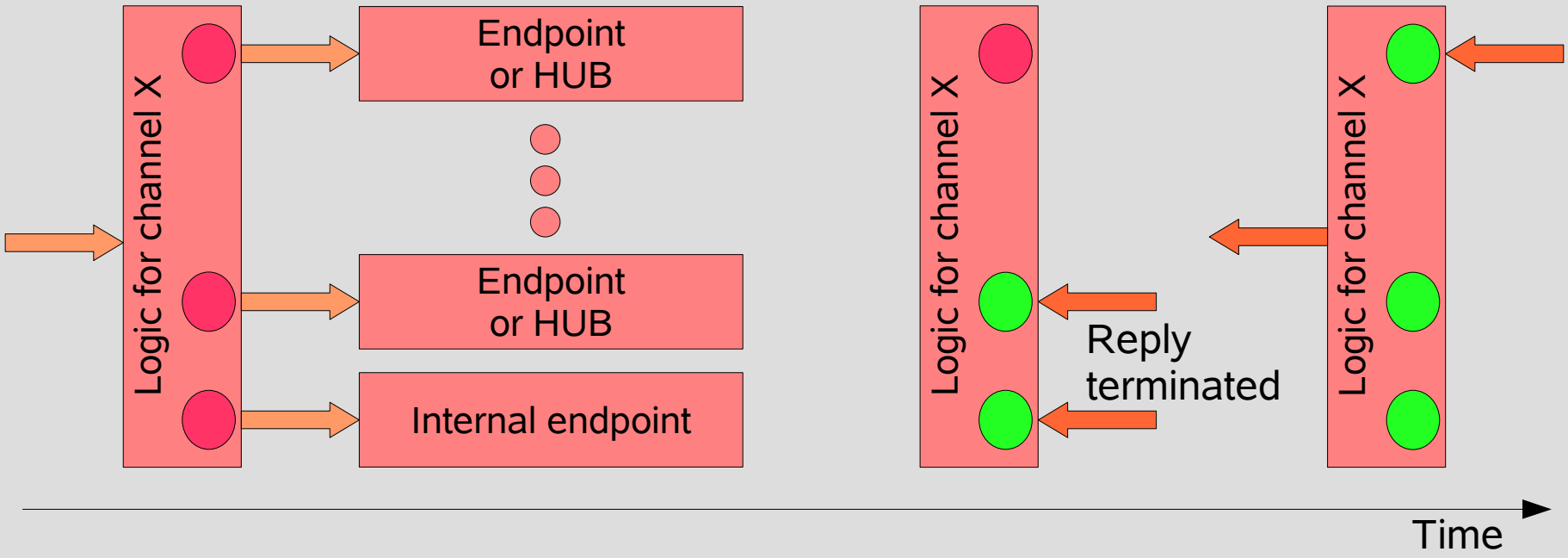
- One channel is e.g. LVL1, LVL2, IPUxxx
- Channels and pathes have *separated* buffers
  - Avoiding deadlocks

Network: Basic Idea

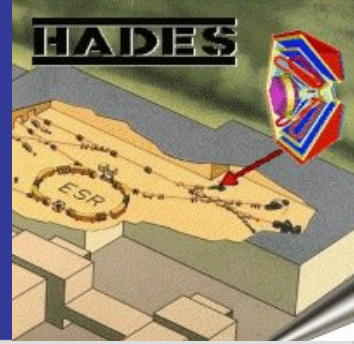


- HADES busy-logic:
  - One channel is blocked until all receivers have released it
    - Old system: wired-or
  - No routing needed
- Realisation in the HUBs:





The Hub



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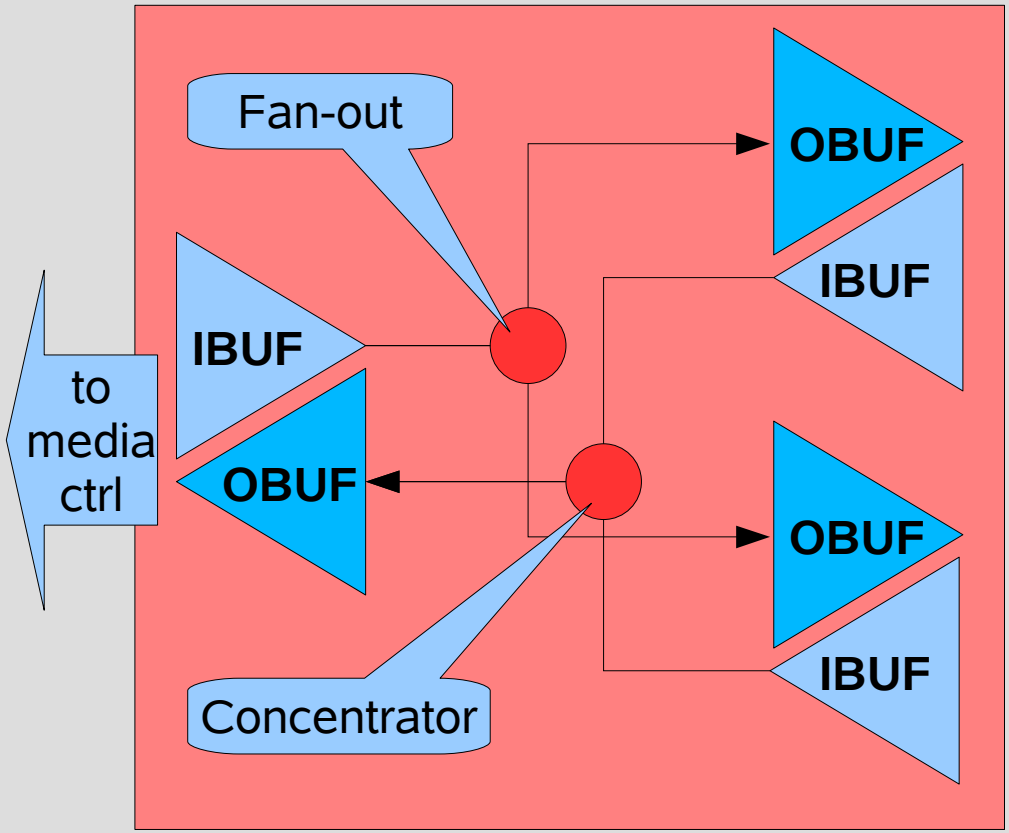
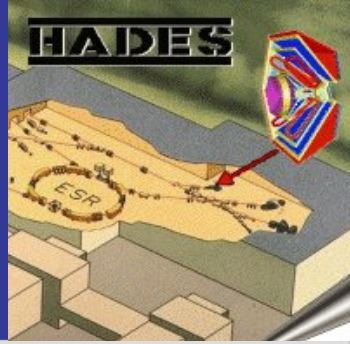
- IBUF
  - A fifo with 2 logical buffers
  - Size not fixed
  - Transmitter has to know the size
- OBUF:
  - Pulling the data from the IBUFs
  - Size normally =0
  - May insert additional control words for handshake logic



The words are pushed into the IBUF, but pulled from the MEDIUM via the OBUF
Speed defined by MEDIUM!

Protocol



- Fixed 64 bit word size. Each word is a:
  - Header (HDR)
  - Data (DAT)
  - Termination (TRM)
  - End-of-Buffer (EOB)
  - Acknowledge (ACK)

For handshake

- Words are forming buffers
  - Matching the *real* IBUF size
    - min 3 words
  - No data loss!
  - 2 buffers may be sent before ACK
- Buffers are forming packets
  - Packet size 1 up to infinity

HDR
DAT
DAT... (for bigger IBUFs)
EOB
DAT
DAT
DAT... or maybe HDRs
TRM

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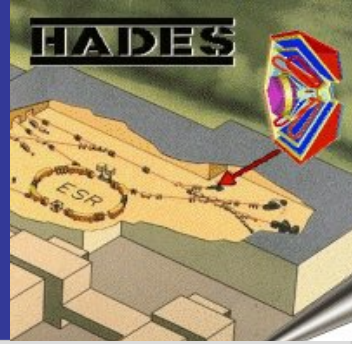
Data Structure



63-56	55-52	51	50-48	47-32	31-16	15-0
res.	CID	P	Type	F1	F2	F3

48 Bit data load

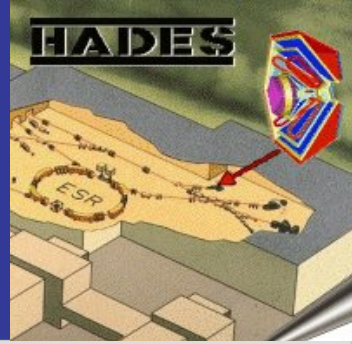
Optional protection via (7,4) Hamming code

- P (Path)
  - 0=INIT, 1=REPLY
- CID (Channel ID)
  - Which of the 16 Channels is used?
  - Allows easy de-multiplexing

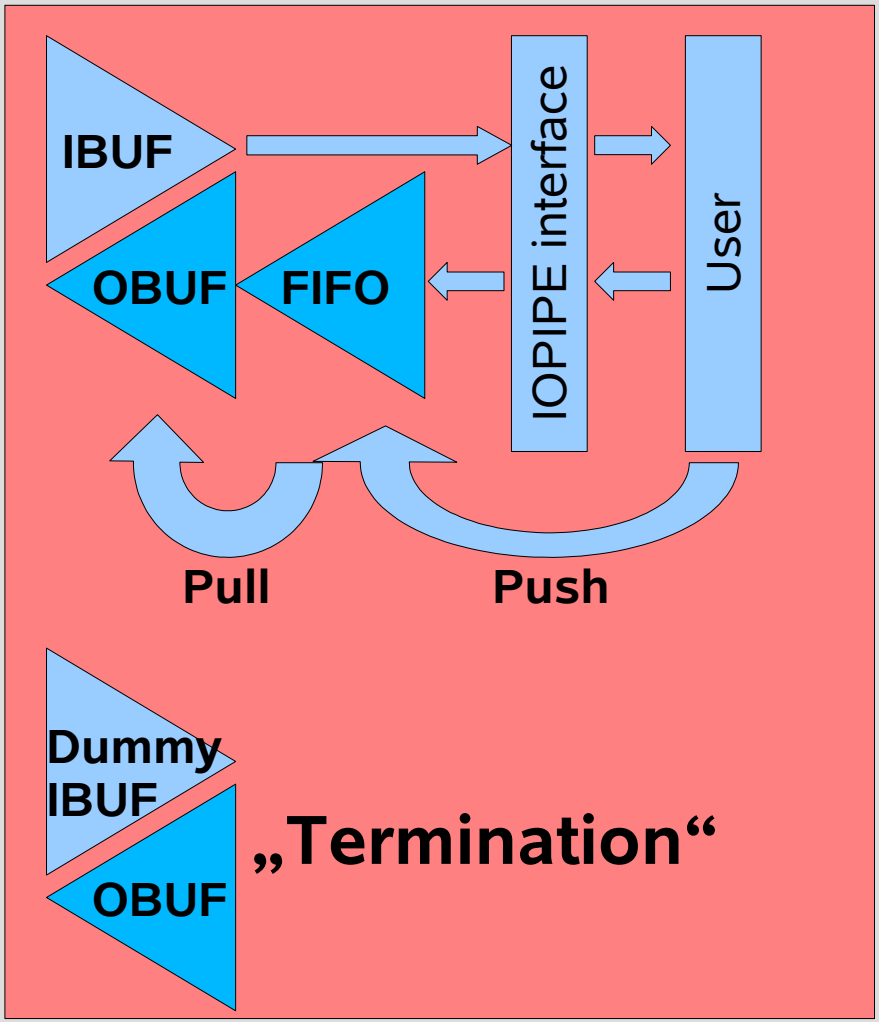
No routing, just for info

Name	Type	Description	F1	F2	F3
HDR	0x1	Initial Transfer	Source adress	Target adress	Bit data
TRM	0x2	Initial Transfer Terminated	Source adress	Target adress	Error pattern
EOB	0x3	End of Buffer	0x0	CRC (optional)	res.
ACK	0x3	End of Buffer	0x1	Length of buffer	res.
DAT	0x4	Data word	Data		

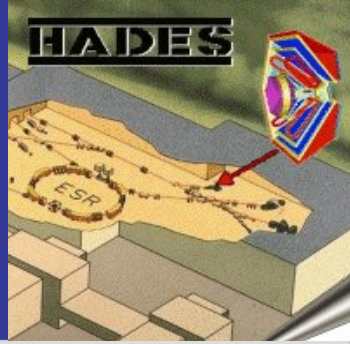
Data Application



- The user should not deal with internals
- Data (one event) may be messed up, but not the network
- IOPIPE: Listen to a fifo, and write to a fifo (only data)
- Additional register control for start the transfer, set error bits, see status etc...



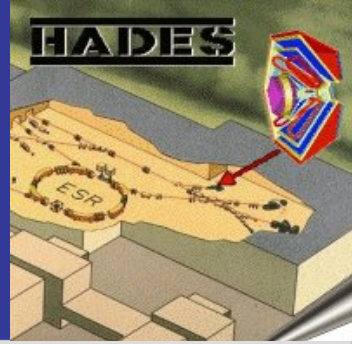
Trigger Bus Application



- HADES trigger bus: One early TRM is enough
  - Bit data for trigger tag, code
  - Error pattern for… well, errors
  - Only broadcasts

Name	Type	Description	F1	F2	F3
HDR	0x1	Initial Transfer	Source adress	Target adress	Bit data
TRM	0x2	Initial Transfer Terminated	Source adress	Target adress	Error pattern
EOB	0x3	End of Buffer	0x0	CRC (optional)	res.
ACK	0x3	End of Buffer	0x1	Length of buffer	res.
DAT	0x4	Data word	Data		

IPU Bus Application



- One Adressing cycle (broadcast)
  - All IPUs are sending data at the same time
- Data merging in the hubs
  - Needs HDR retransmit
  - In other words: Buffers may be

HDR (IPU1)

DAT..

HDR (IPU2)

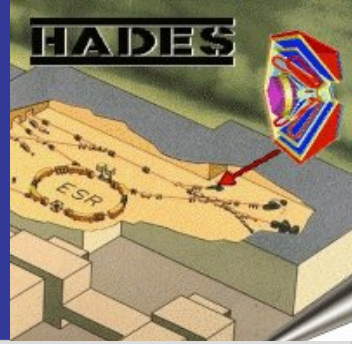
DAT...

HDR (IPU1)

DAT...

Name	Type	Description	F1	F2	F3
HDR	0x1	Initial Transfer	Source adress	Target adress	Bit data
TRM	0x2	Initial Transfer Terminated	Source adress	Target adress	Error pattern
EOB	0x3	End of Buffer	0x0	CRC (optional)	res.
ACK	0x3	End of Buffer	0x1	Length of buffer	res.
DAT	0x4	Data word	Data		

Media Layer Interface



Medium

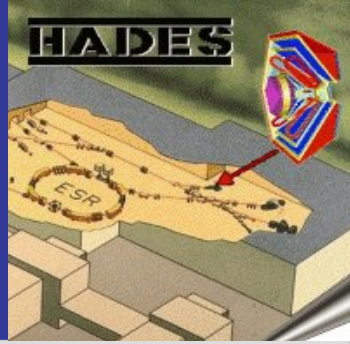
Line	Decription
INT_DATAREADY_OUT	Data word is reconstructed and ready to be read out by the internal logic
INT_DATA_OUT[0...55]	Data word
INT_READ_IN	Internal logic is reading from the FIFO
INT_ERROR_OUT[0..2]	Status bits
MED_DATAREADY_IN	Data word is offered by the internal logic or FIFO
MED_DATA_IN[0...55]	Data word
MED_READ_OUT	Media interface reads a word
MED_ERROR_IN[0..2]	Status bits

Physical Layer

Network Protocol Layer

- Hides the current implementation of the medium from the NPL

More Features



- Adresses: 12 bits are enough for the TRB system
  - 4 Bits could be used as a minor number
  - E.g. add-on board, virtual componants...
- Also protocol for the TRB<->AddOn communication
- Channel 15 should emulate a remote bus (part of the Data Layer)
  - the way hubs are programmed
  - basic state machine states should be readable
    - Common monitoring from a central place
- A lot of spare word types
  - Open for future extensions

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