Status of the GET4 TDC Development

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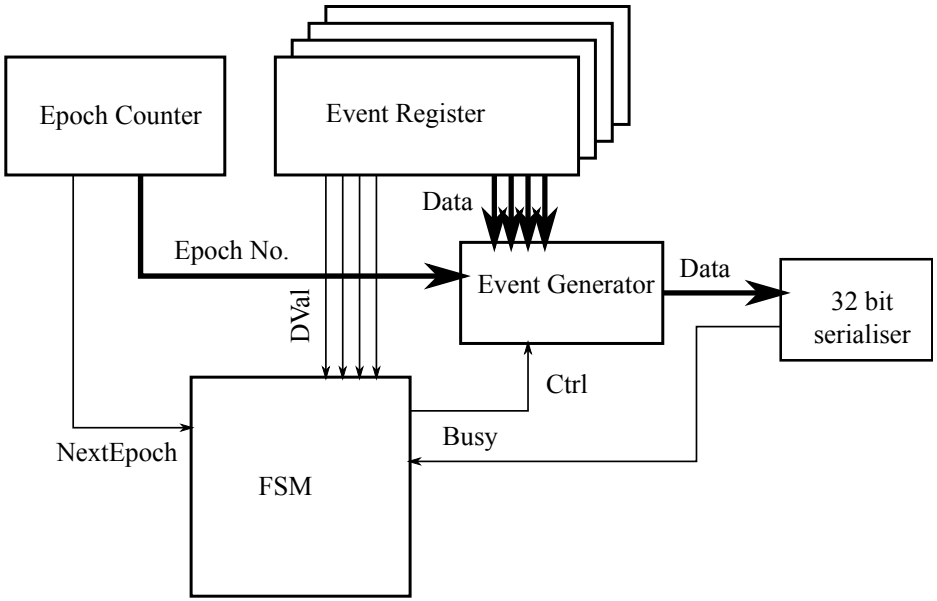
Outline

Missing Epoch Events

- Observed effect:
  Simultaneous hits on more than two channels in a small time window at the end of an epoch lead to a missing epoch event.
- Status:
  The effect could be reproduced in simulation. The reason was identified as a wrong state transition in the finite state machine which sends data to the serialiser.
  The state machine VHDL code was modified and works now correctly in simulation.

Missing Epoch Events



Related states:

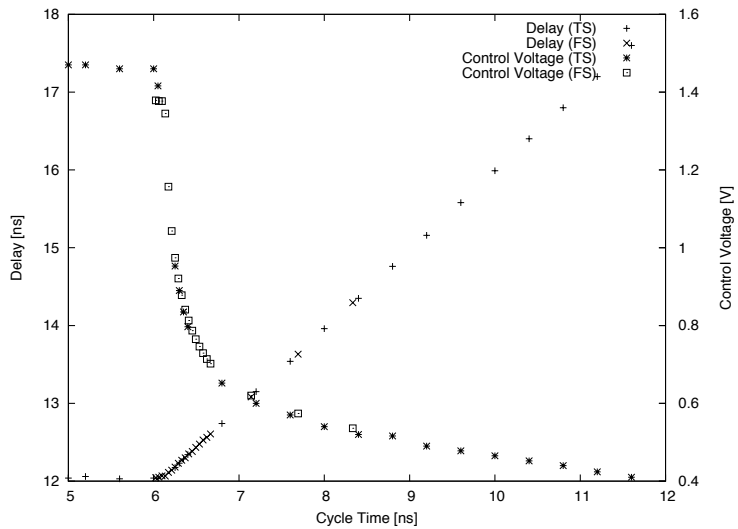
- WaitTXData
- TXData
- WaitTXEpoch
- TXEpoch

- In TXData state Event generator sends event data to serialiser, serialiser will become active on next clock cycle
- If *NextEpoch*-Signal arrives in this state FSM goes to TXEpoch state as Busy is currently not active
- On next clock cycle event generator sends epoch event to a busy serialiser
- $\Rightarrow$ On *NextEpoch*-signal during TXData FSM always has to go to WaitTXEpoch state!

DLL Lock Range

Retrospection

- When the TDC core development took place CBM system clock was 250 MHz (given by clock frequency of 2.5 GBit Serdes)
- DLL design with 50 ps stage delay was tradeoff between a reasonable safety margin and the best timing precision
- For DLL lock: $T_{min} = 6.14$ ns $\rightarrow f_{max} = 162.8$ MHz
- Later MPW runs showed large process variations between runs



DLL Lock Range

Retrospection, Change in CBM DAQ Design

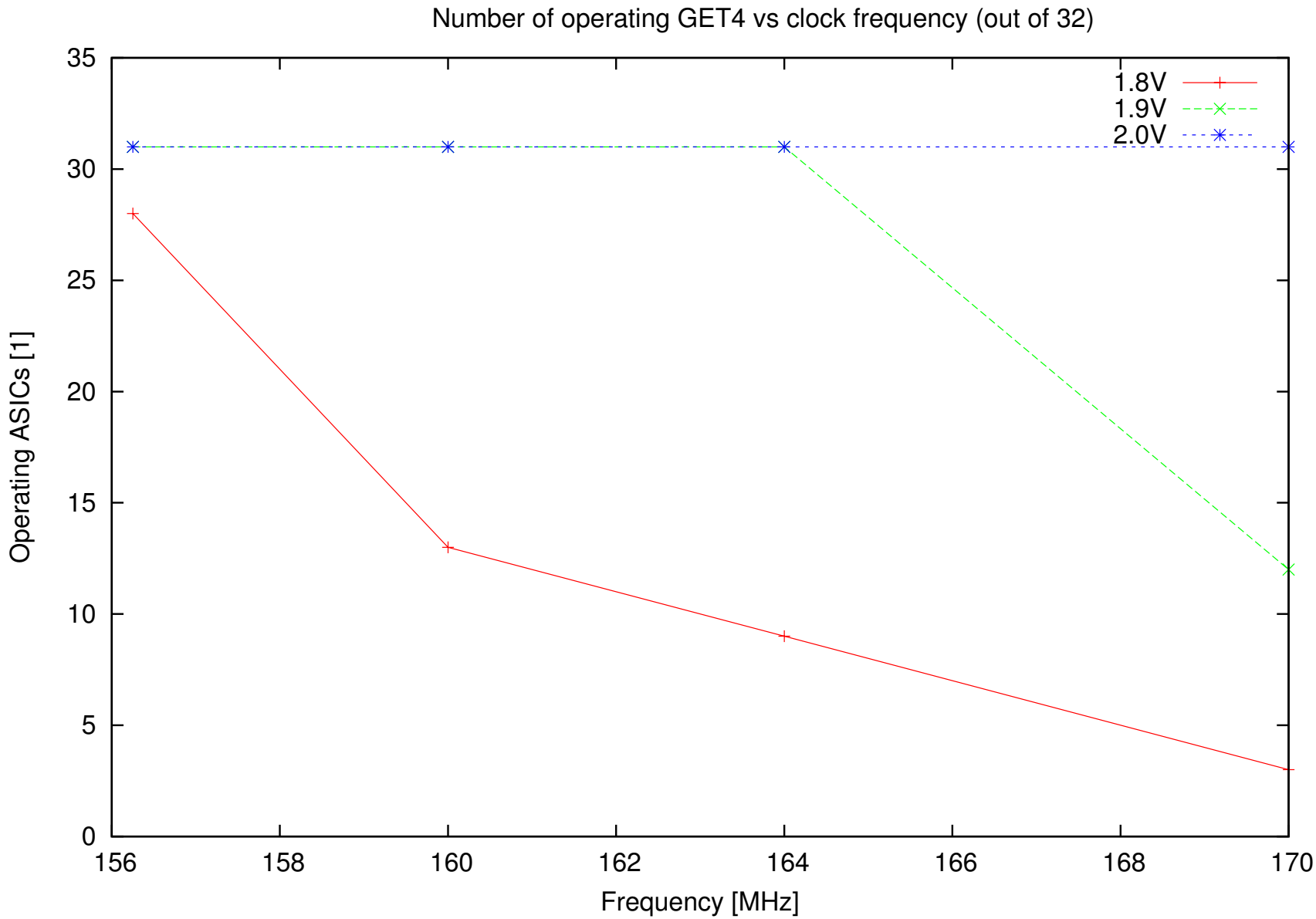
- In 03/2014 CBM decided a DAQ architecture change from CBMnet $\rightarrow$ GBTX
- GBTX A radiation hard high speed communication ASIC developed at CERN
- GBTX clock frequency: LHC bunch crossing frequency $f_{LHC} = 40,0789$ MHz. Available data rates are: $f_{br} = 1, 2, 4, 8 \cdot f_{LHC}$. for $N = 4$: $f_{br} = 160.3156$ MHz
- GBTX uses a VCXO based PLL with quartz crystal implemented in chip package which defines operating frequency. Crystal frequency could be adapted at the chip order.
- Our proposal was: Going to GBTX operating frequency of 39.0625 MHz. CBM decided to go to 40 MHz, order in 12/2014
- $\Rightarrow$ GET4 now has to work in a 160 MHz environment

Lock range

- In first testchips upper limit of lockrange was 164 MHz
- First problems occured in V 1.10: Significant part of Chips does not lock at design frequency
- Wide spread of DLL speed due to process variations
- Four possible solutions
  - Selection of ASICs $\Rightarrow$ bad yield
  - Increasing of supply voltage $\Rightarrow$ possibly reduction of lifetime, ± 10 % seems to be safe
  - Reduction of clock frequency $\Rightarrow$ Introduces a second clock domain
  - Reducing number of delay elements in DLL

DLL Lock Range

GET4, Operating Frequency, Power Supply



Fake Edges

- First observation: TOT, Overwrite and Discard errors in 32 bit mode data stream
- Errors disapear with higher supply voltages
- possible explanation: Missing or additional edges from TDC core
- First suspect: timing of data transfer from TDC core to readout logic
- Jochen looked for unpaired edges in 24 bit mode in lots of tests
- Typical pattern was found by Jochen

Fake Edges

Observation: If a well defined bin was hit with a trailing edge an additional leading edge close to this trailing edge is seen in the data stream

Board	Channel	L1	L2	T1
1	7	118	67	70
3	30	21	99	102
7	16	36	113	114
7	17	36	113	114
7	18	36	113	114
7	19	36	113	114
8	4	38	115	118
12	22	105	55	62

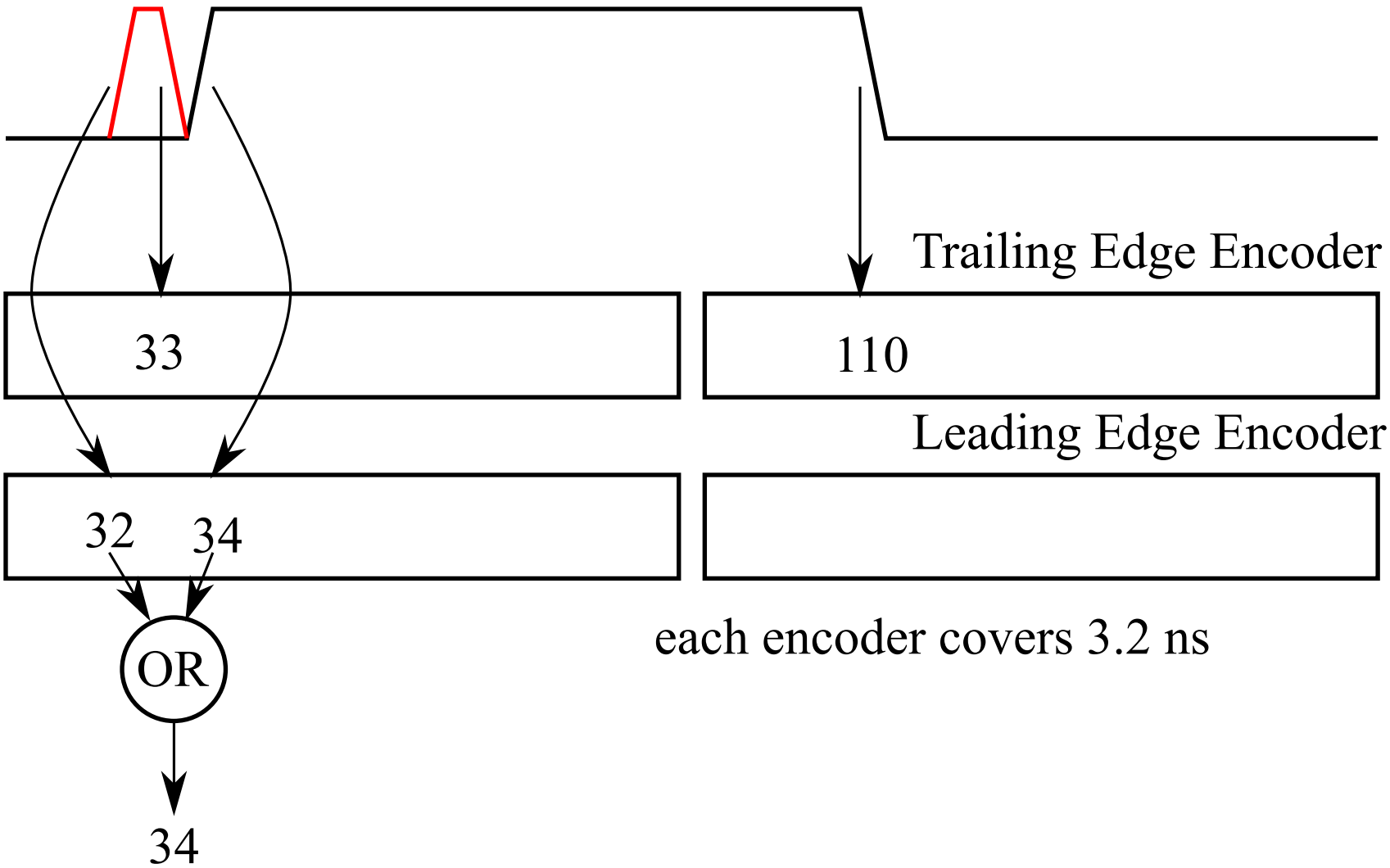
Fake Edges

Similar Observation for Trailing edges

Board	Channel	L1	T1	T2
2	5	46	39	115
5	3	102	101	51
5	25	110	103	55
6	22	34	33	110
6	23	34	33	112
8	7	18	17	94
8	16	110	107	57
8	26	30	23	101
11	7	30	29	106

FakeEdges

Explanation: Bubble Problem



FakeEdges

Options for solution

- Modifiing Edge detector in TDC core
  - Currently uses a history of one bin, could be modified to a history of up to three bins
  - Modification of full custom designed TDC core $\Rightarrow$ leads to the need of large redesigns of the TDC core
- Detecting in the digital read out
  - Clear signature when edges are time sorted:
    - Trailing edge without previous leading edge
    - Two consecutive leading edges
  - Edges of same type are allready time sorted
  - Close leading and trailing edges might be inverted $\Rightarrow$ sorting is required
  - Modification of time over threshold calculator

Engineering Run

- For end of January a common engineering run of STS-xyter, PADI and GET4 was planned.
- STS xyter is delayed
- 10000 channels of GET4 and PADI are needed for setup at STAR
- GET4 design for STAR is ready for tape out.