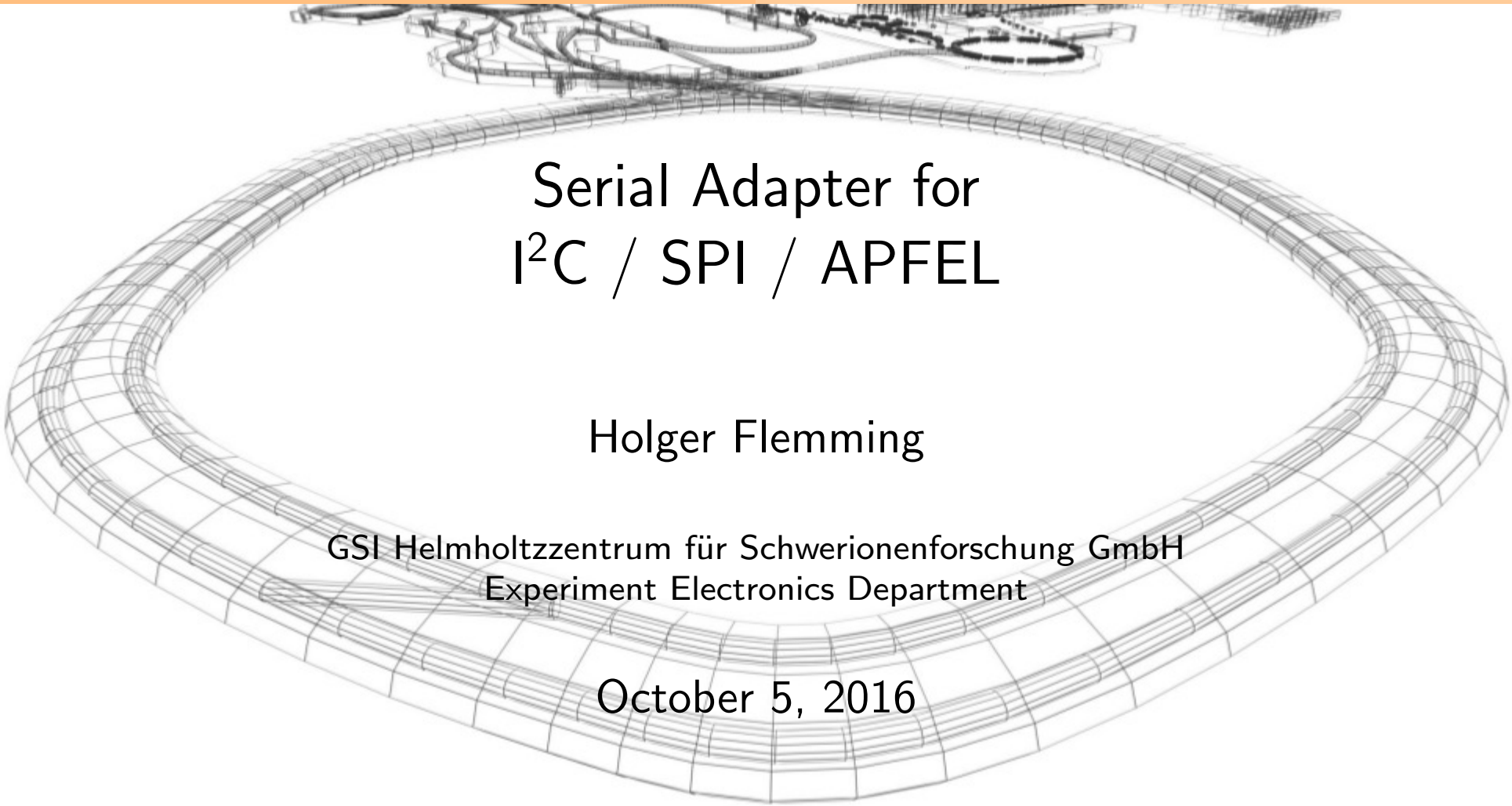

Serial Adapter for I²C / SPI / APFEL

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Experiment Electronics Department

October 5, 2016

Outline

Motivation

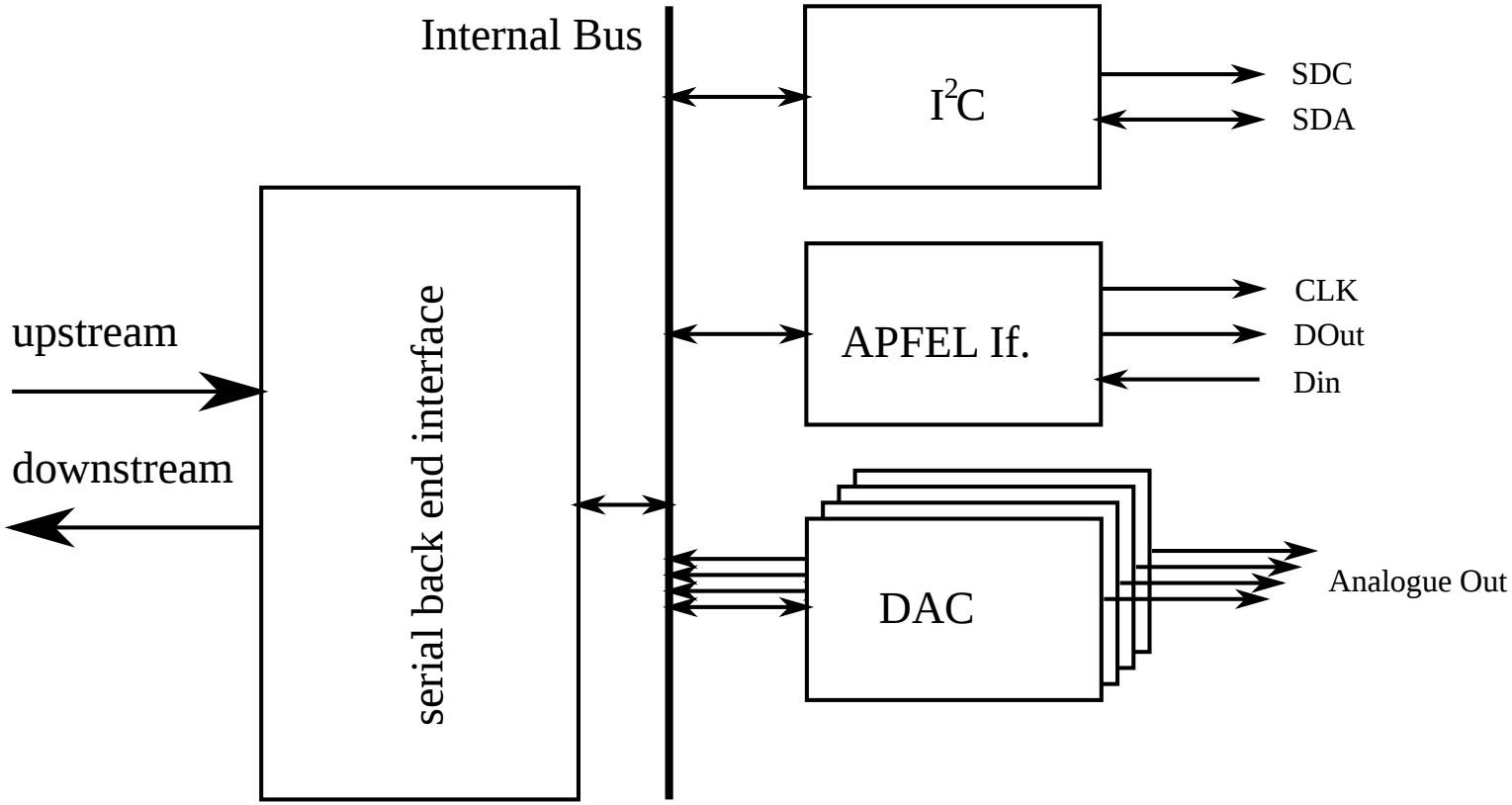
- Currently two different serial interfaces are foreseen to be used inside the barrel:
  - I^2C for High voltage DACs
  - APFEL serial configuration interface
- Both interfaces use single ended lines
  $\Rightarrow$ need ground connection $\Rightarrow$ Risk of ground loops
- Both interfaces are not compatible $\Rightarrow$ Requires additional cabling inside the magnet.

Wish for an adaptor circuit with additional analogue features raised up.

$\Rightarrow$ Integration of 10 bit DACs for HV adjustment.

Proposal

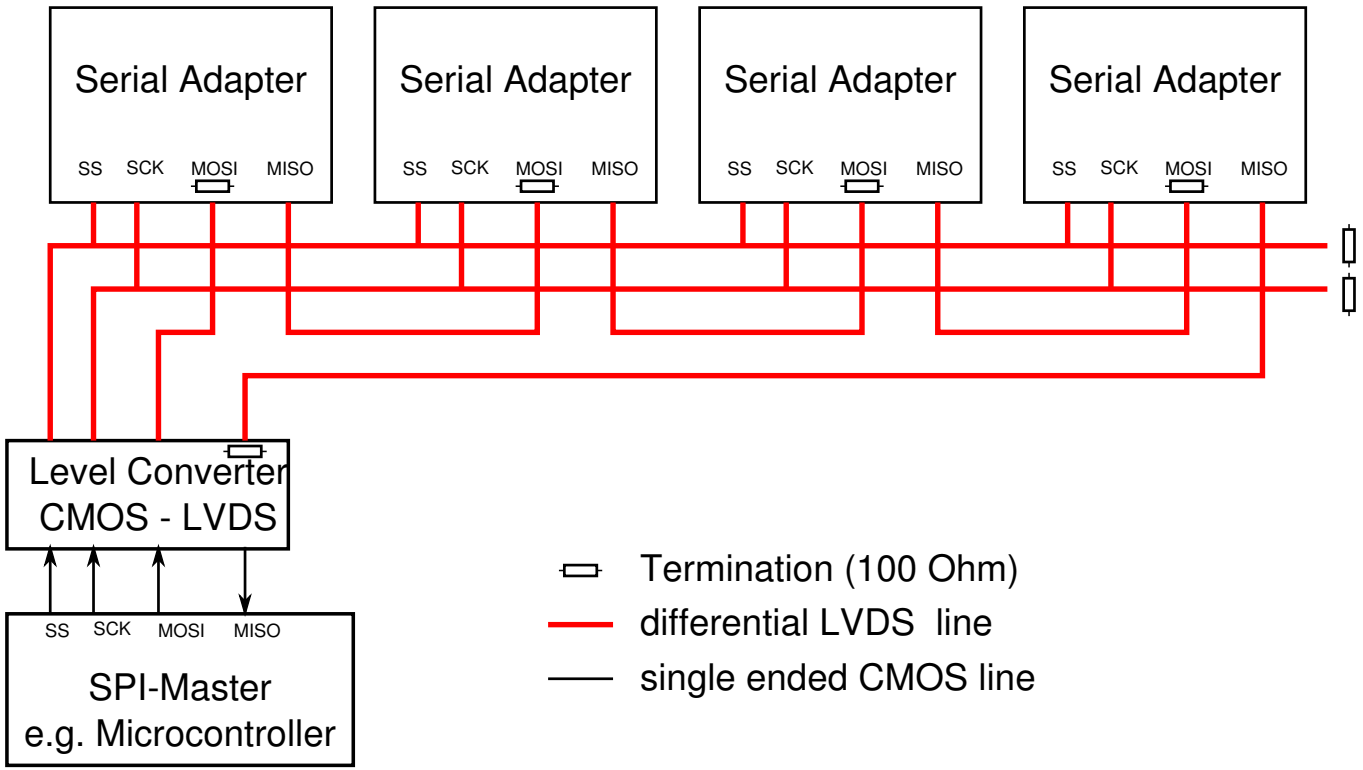
Build an adaptor circuit with a common back end and front ends for I^2C, SPI and APFEL serial configuration interface



Proposal

Back end

Using a daisy chained SPI interface



Proposal

Front end

- I^2C
- APFEL configuration interface
- 8 Analogue DAC outputs
- 3 Bit multi purpose CMOS IO (each pin configurable as input or output)

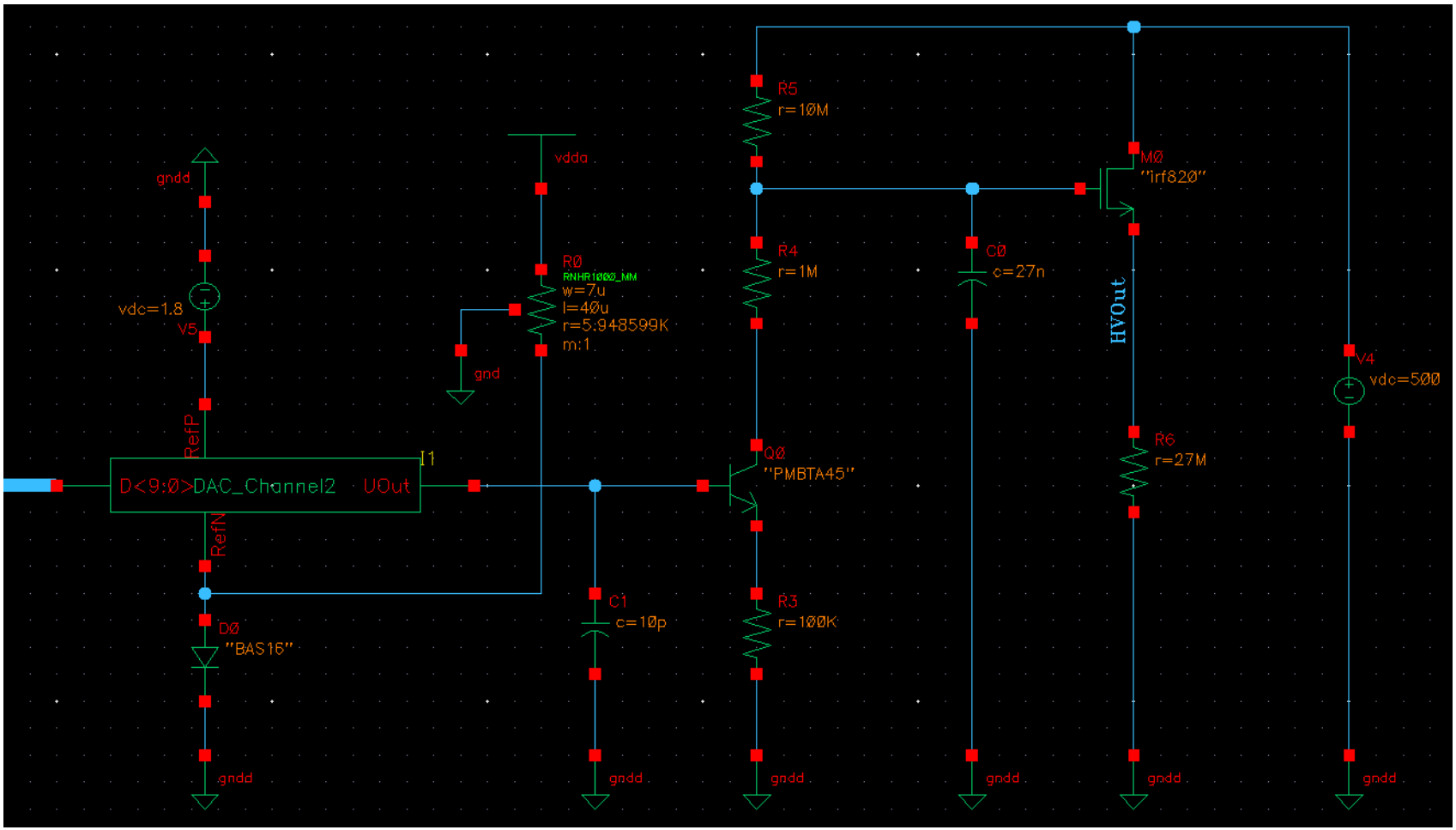
Proposal

IO Pins

Power (1.8V Core, 3.3V IO)	4
Back end SPI – LVDS	8
Power On Reset (Out)	1
Reset	1
I^2C	2
APFEL Interface	3
DAC Outputs	8
DAC Reference, low end	2
3 Bit Multi Purpose IO	3
Sum	32

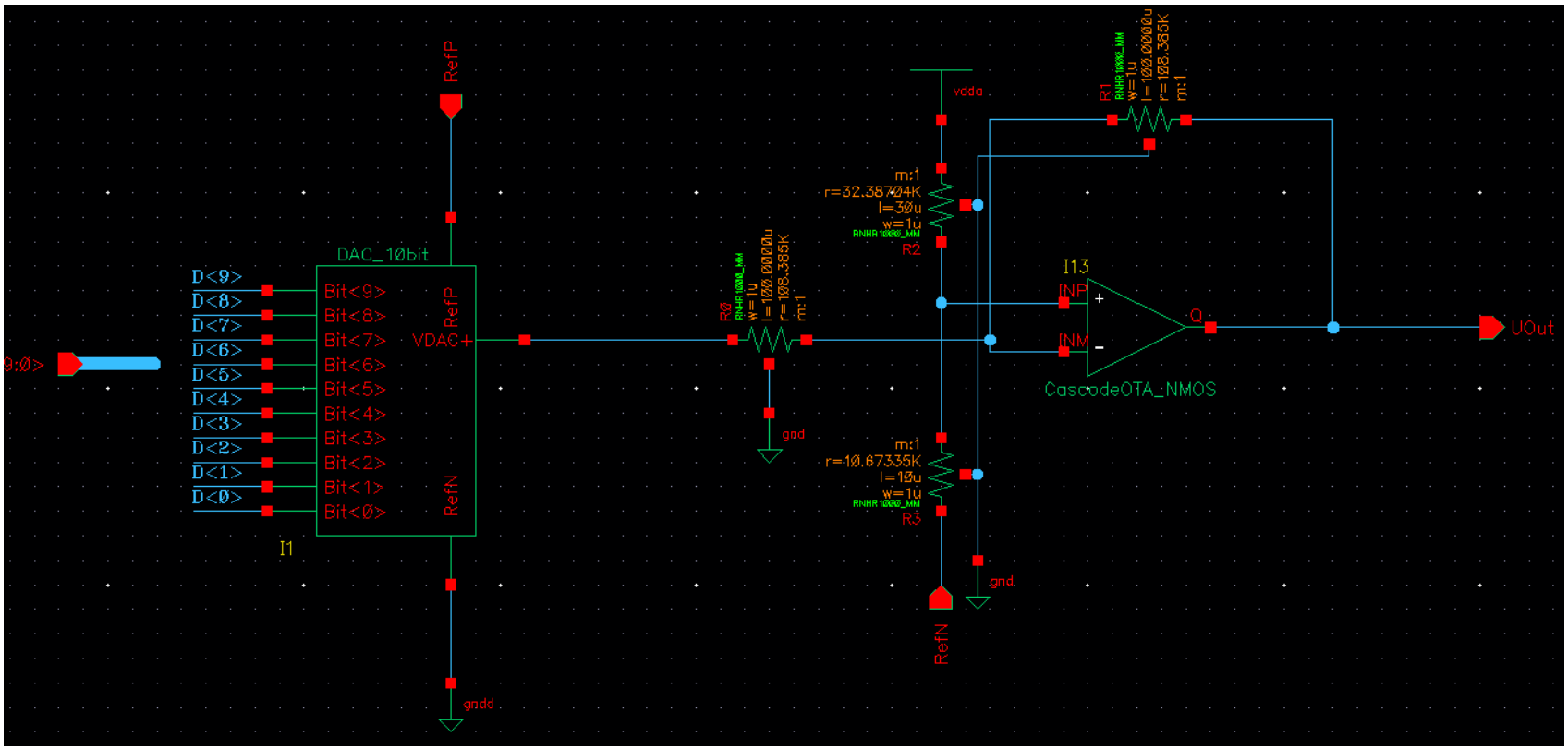
$\Rightarrow$ Fits into QFN32 package with 5 by 5 mm^2 !

HV Adjustment Architecture



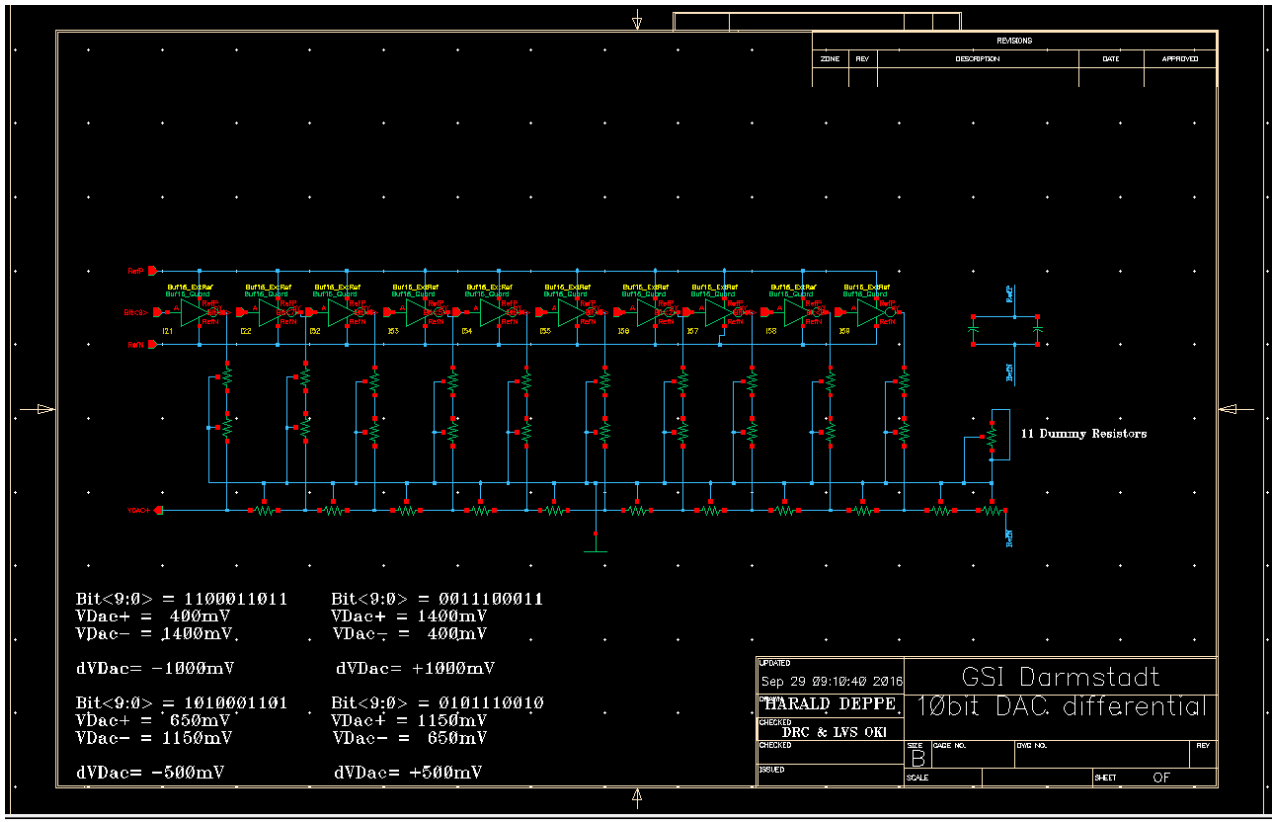
HV Adjustment Architecture

DAC driver



HV Adjustment Architecture

DAC Architecture

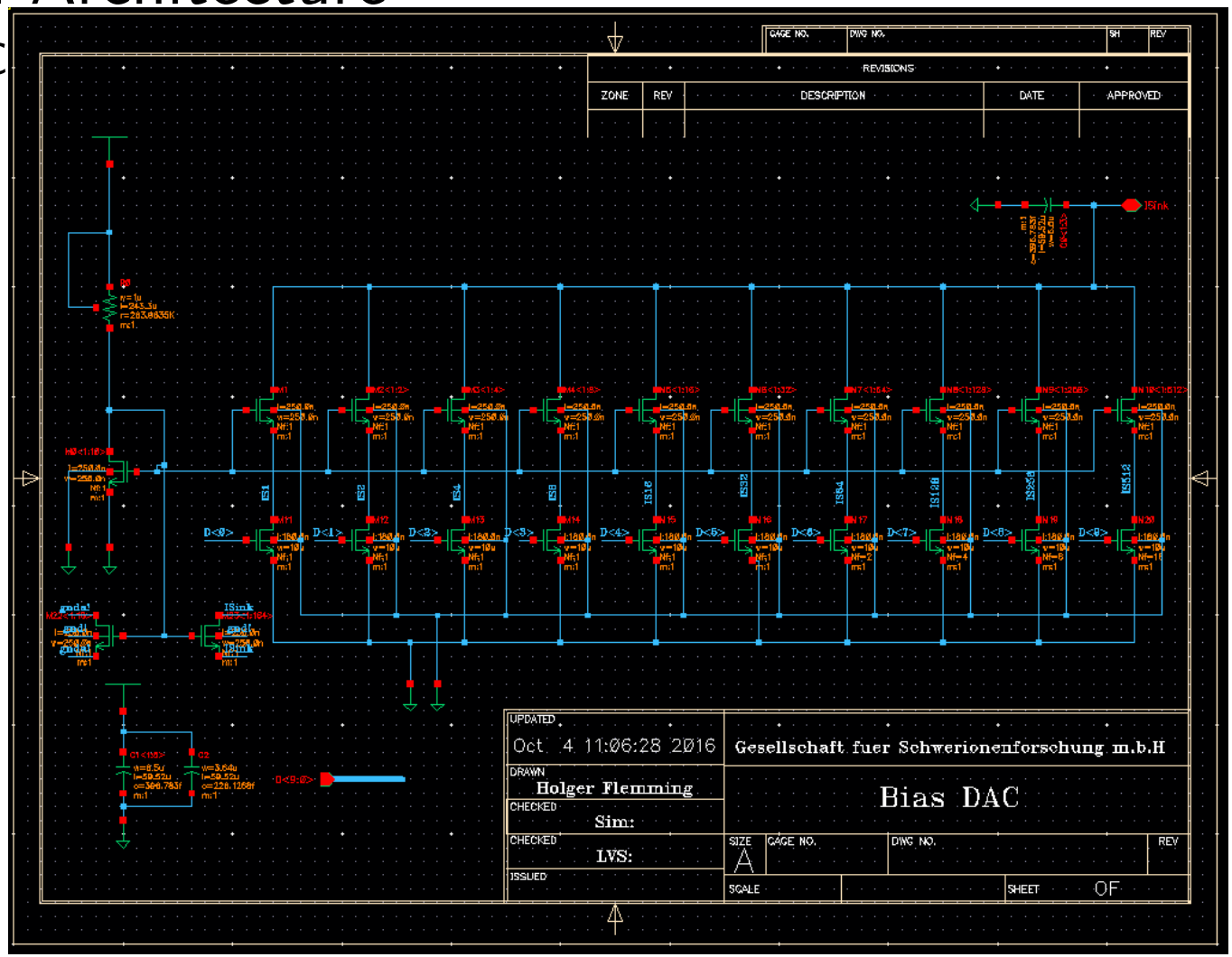


HV Adjustment Architecture

Simulation Results

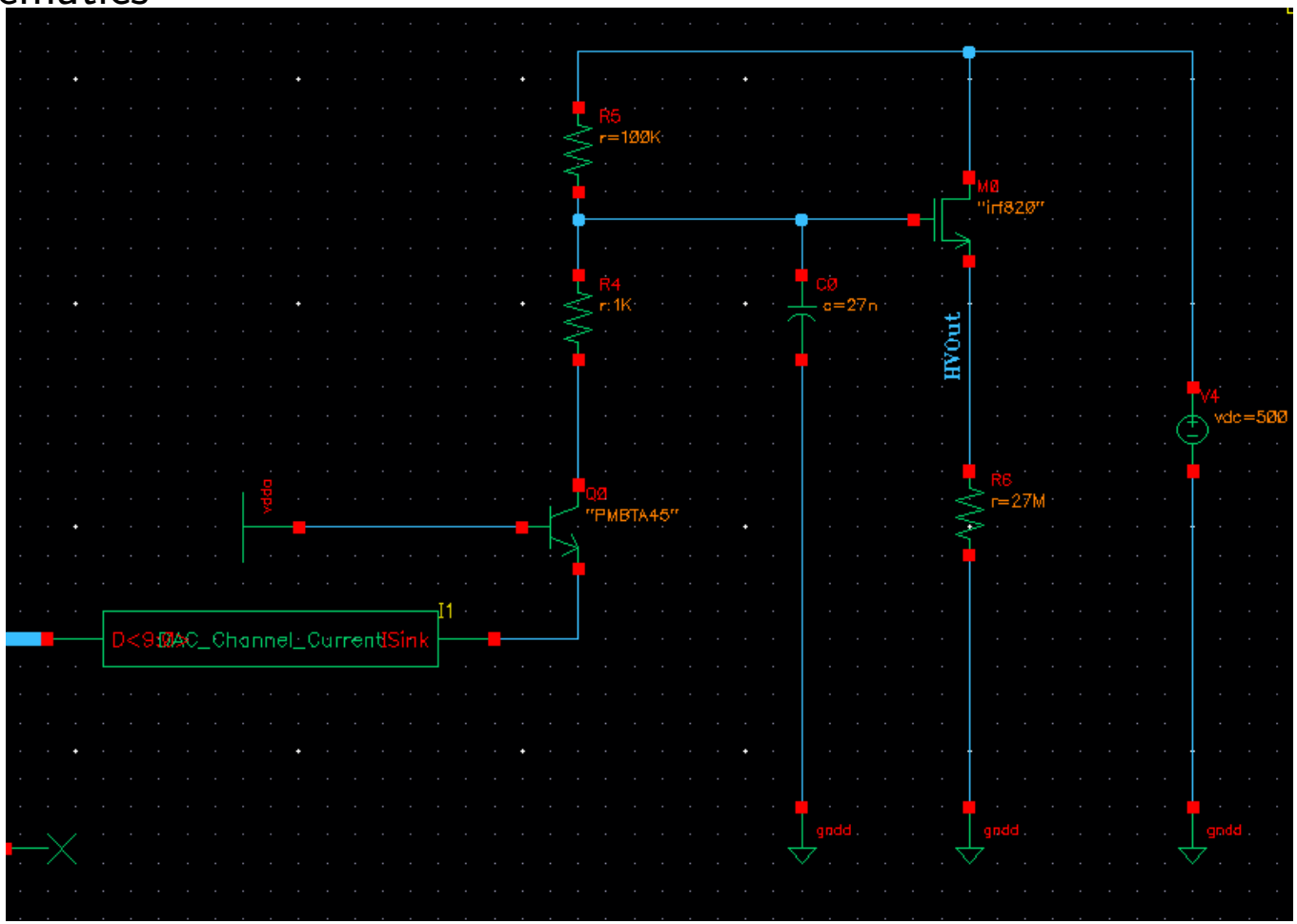
Optional Architecture

Current DAC



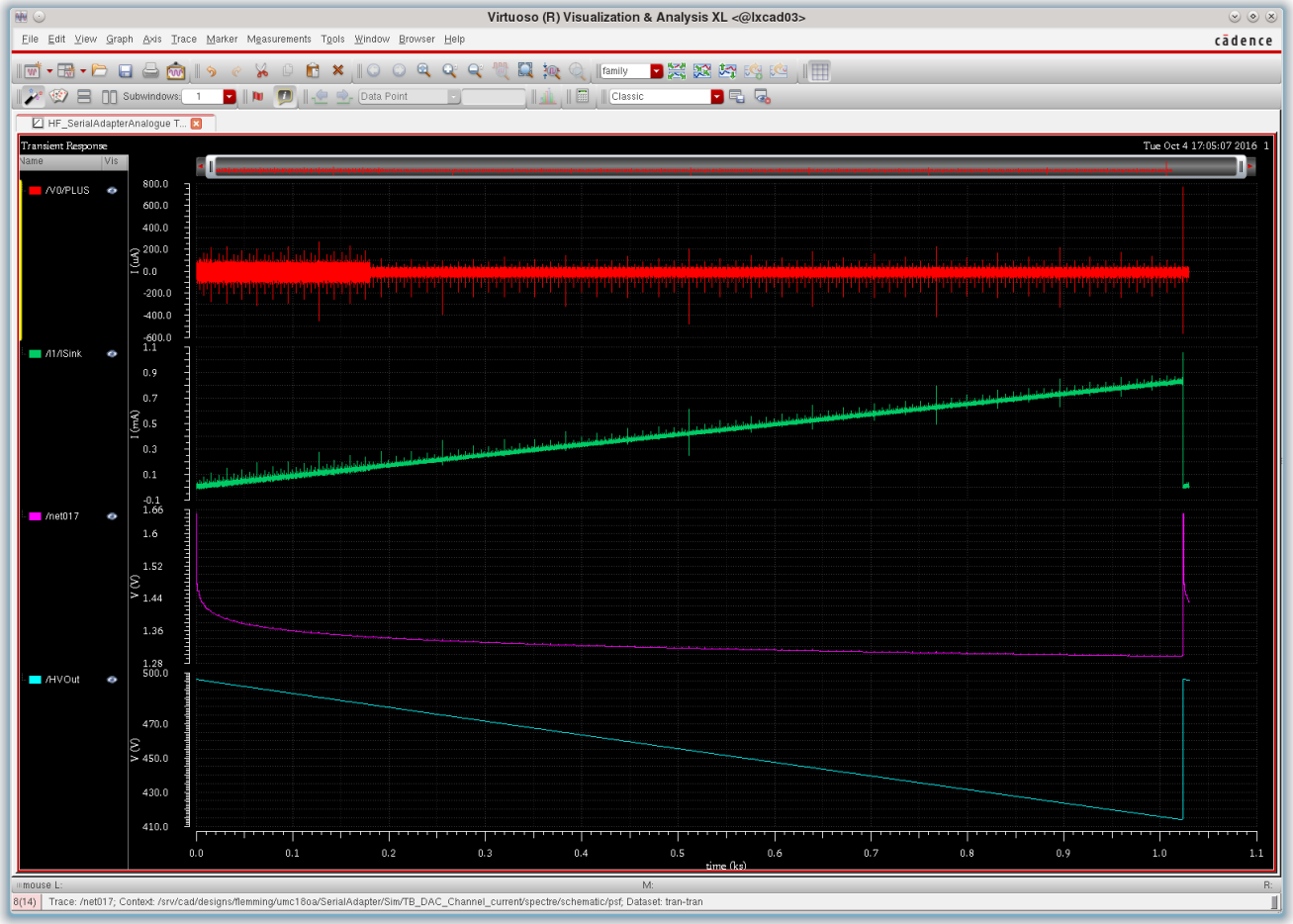
Optional Architecture

External Schematics



Optional Architecture

Simulation Results



Status and Schedule I

- Reuse of available Analogue blocks ⇒ Full digital design based on VHDL code with Analogue macro blocks
- VHDL Code is almost completely written
- Synthesis and Place & Route scripts are prepared
- Still needed:
  - Final Analogue Design
  - More detailed simulations
  - Analogue macro block has to be implemented in Floor planning script
  - Final syntheses and Place & Route Run

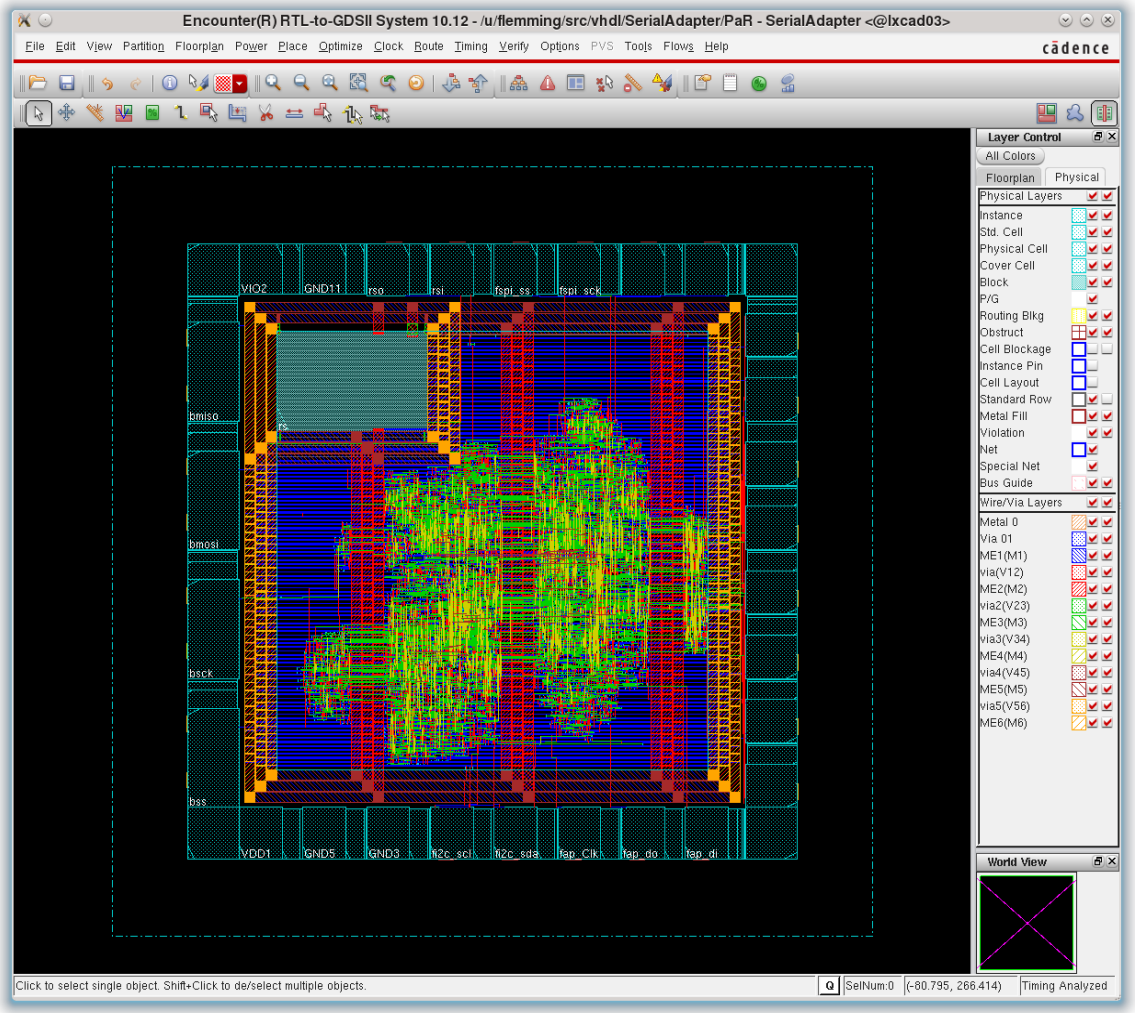
Status and Schedule II

- Estimation of required development time:
  - Analogue Design $\approx$ 3 weeks
  - VHDL Simulation: $\approx$ 2 weeks
  - Synthesis and Place & Route: 1 week
- Next available tape out: November 28th / December, 5th 2016
- Delivery of Silicon in March 2017
- Packaged chips available spring 2017

Costs

Number of Chips		Total costs	Packaging	Cost/chip
30	(min. number)	€6320	€2500	€294
180	(one slice)	€12820	€2500	€85.11
270		€32200	€2500	€128.52
4050	(full barrel)	€50650	€5000	€13.75

Chip Layout


Encounter(R) RTL-to-GDSII System 10.12 - /u/flemming/src/vhdl/SerialAdapter/PaR - SerialAdapter <@lxcad03>
File Edit View Partition Floorplan Power Place Optimize Clock Route Timing Verify Options PVS Tools Flows Help
cadence
Layer Control
All Colors
Floorplan
Physical
Physical Layers
Instance
Std. Cell
Physical Cell
Cover Cell
Block
P/G
Routing Blkg
Obstruct
Cell Blockage
Instance Pin
Cell Layout
Standard Row
Metal Fill
Violation
Net
Special Net
Bus Guide
Wire/Via Layers
Metal 0
Via 01
ME1(M1)
via(V12)
ME2(M2)
via2(V23)
ME3(M3)
via3(V34)
ME4(M4)
via4(V45)
ME5(M5)
via5(V56)
ME6(M6)
World View
VIO2
GND11
rso
rsi
fspi_ss
fspi_sck
bmiso
bmosi
bsck
bss
VDD1
GND5
GND3
fi2c_scl
fi2c_sda
fap_Clk
fap_do
fap_di
Click to select single object. Shift+Click to de/select multiple objects.
SelNum:0
(-80.795, 266.414)
Timing Analyzed

Backup

Digital Design Flow