HADES Triggered/TDC Readout Board TRB

Outline

- Applications for TRB
- Architecture
- Details of Implementation
- Results
- Future

Applications

EU-FP6 Construction Contract

- Resistive Plate Chamber / **RPC**
  - Timing (Time of Flight)
  - correction with amplitude (walk correction)
- Pion Hodoscopes
- Forward Wall

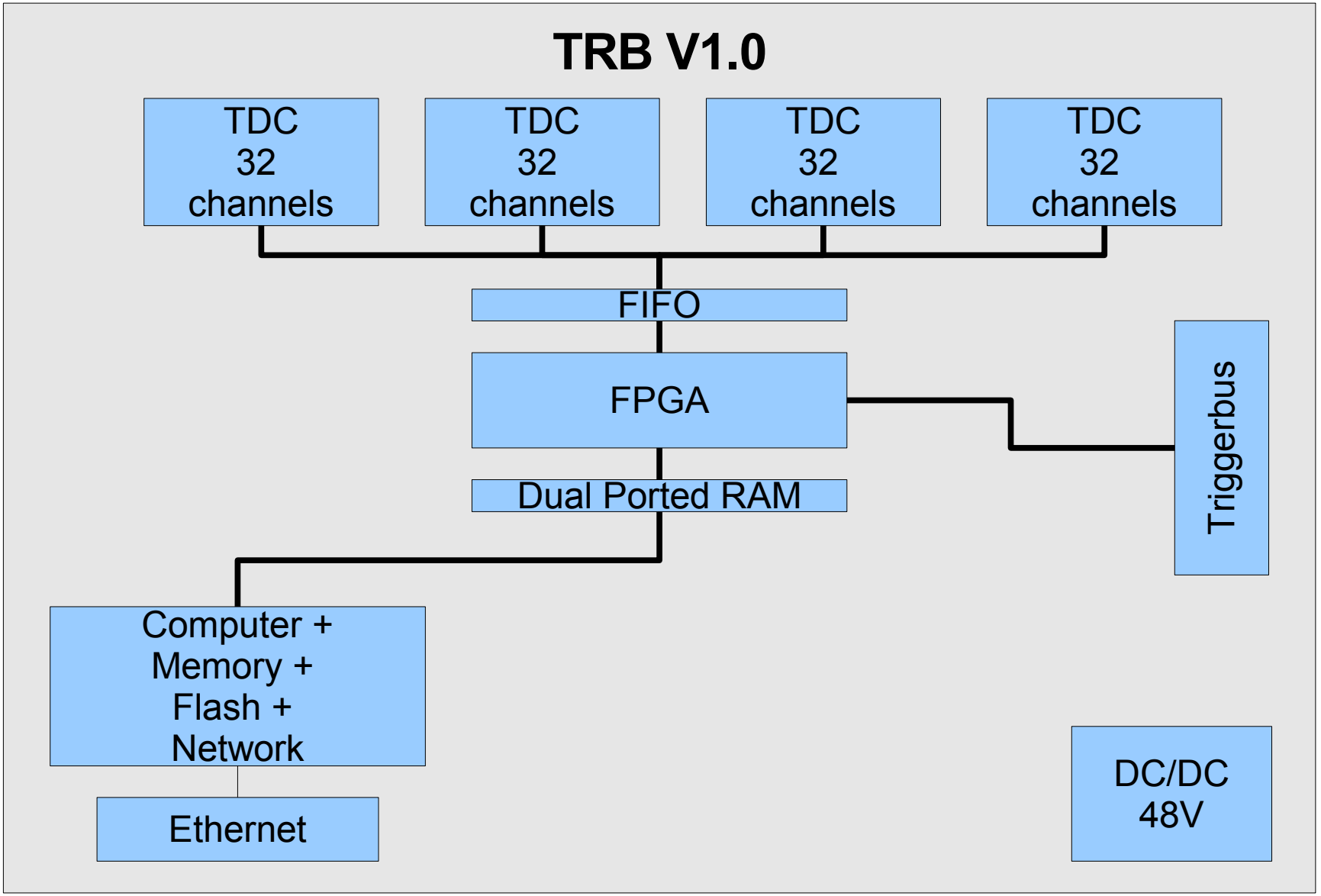
BMBF

- TOF Readout / Trigger
- RICH Readout / Trigger
- MDC Readout / Trigger

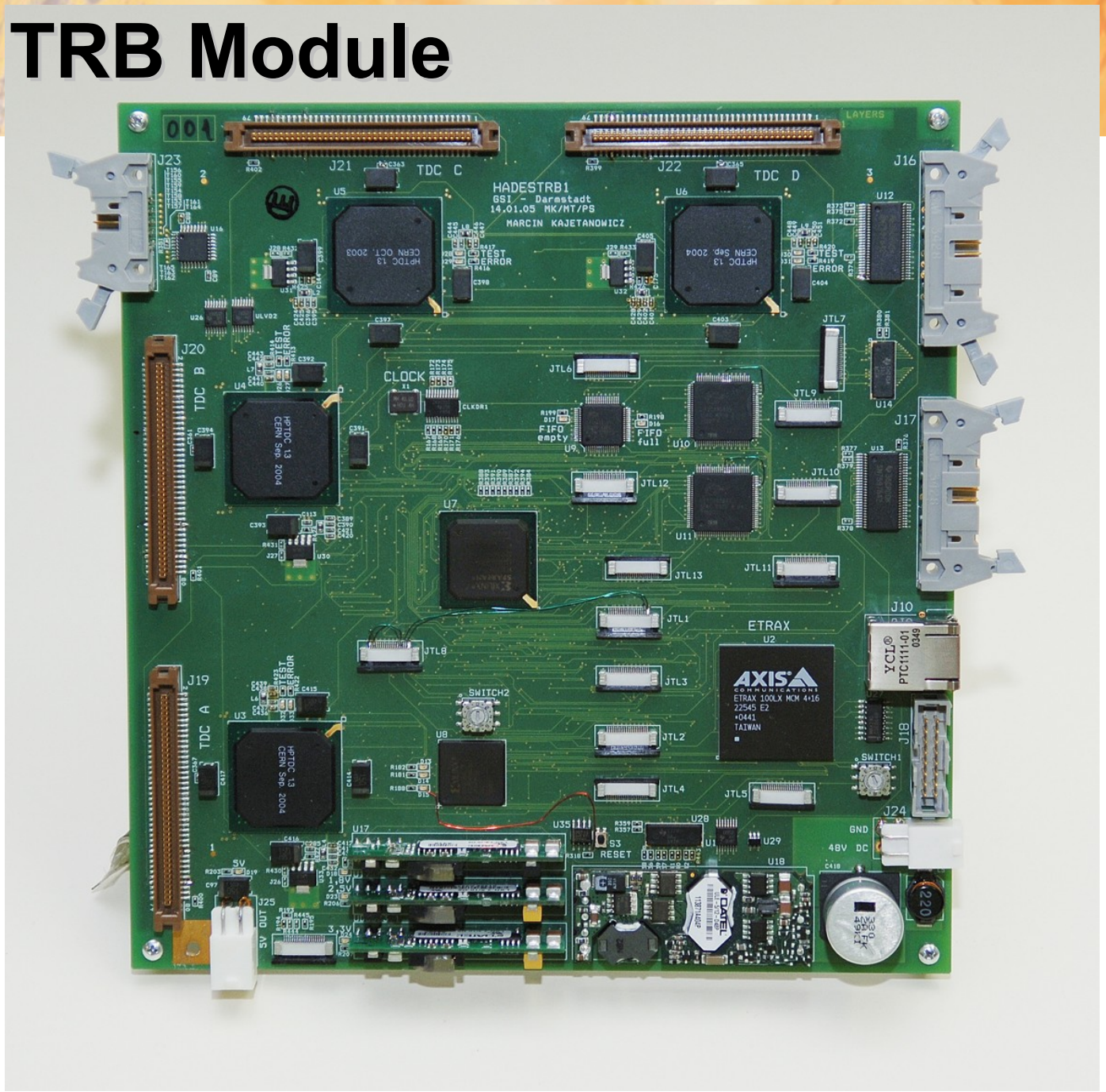
Features/Requirements for RPC

- At the detector, short signal cables
- Purely digital, ADC information is encode in Time-over-Threshold
  - No delays required, no ADCs needed
  - HPTDC from CERN
- LVL1 and LVL2 pipes at the FEE
- Readout and data transport on one board, **no VME**
- Avoid „*Low Voltage Power-Supply Nightmare*©“ (high currents over long cables: Ohm's Law, Inductive-effects)
  - 48V DC/DC, telecom standard
- Data Reduction/Feature extraction on the same board

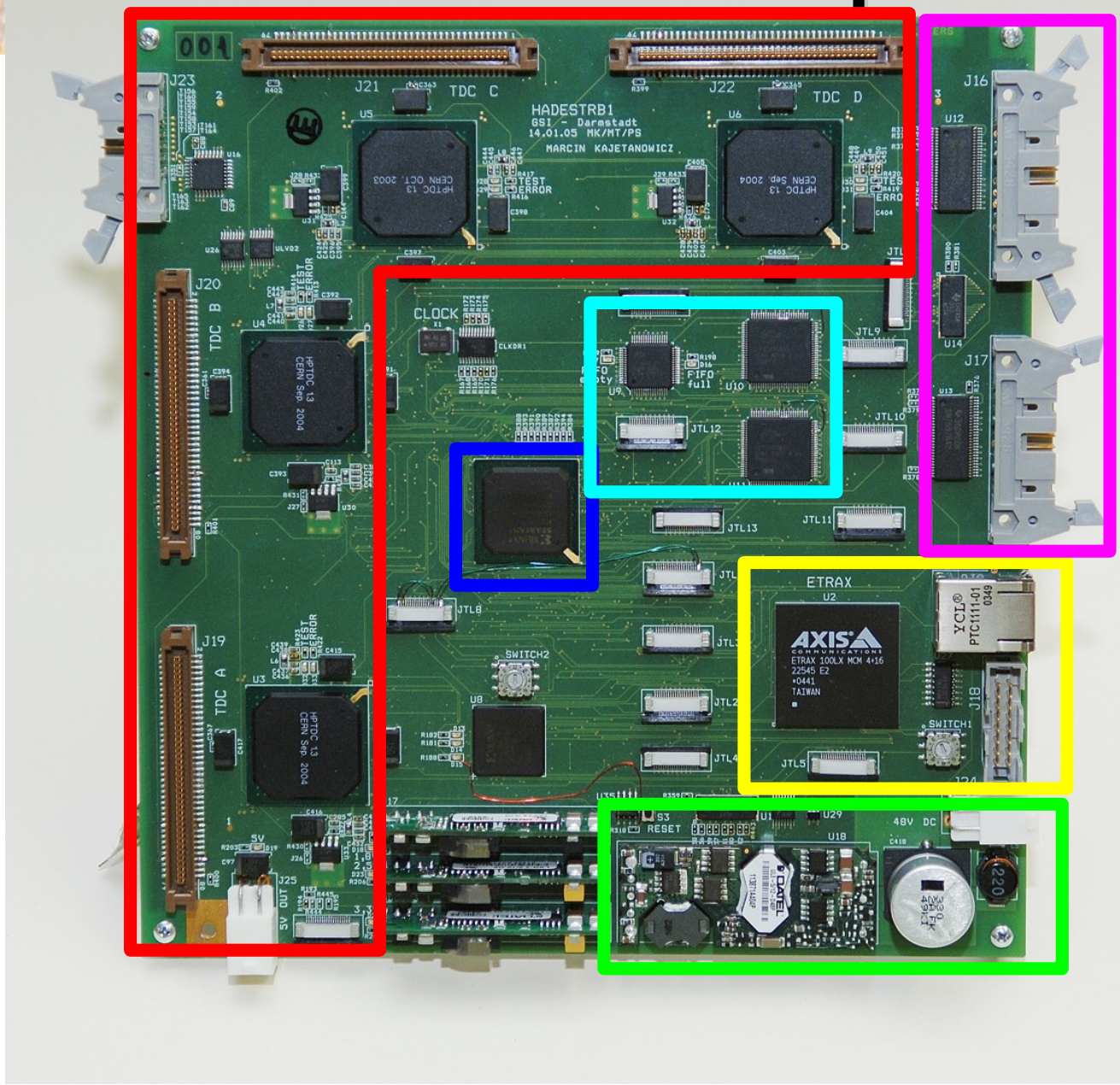
Architecture



TRB Module

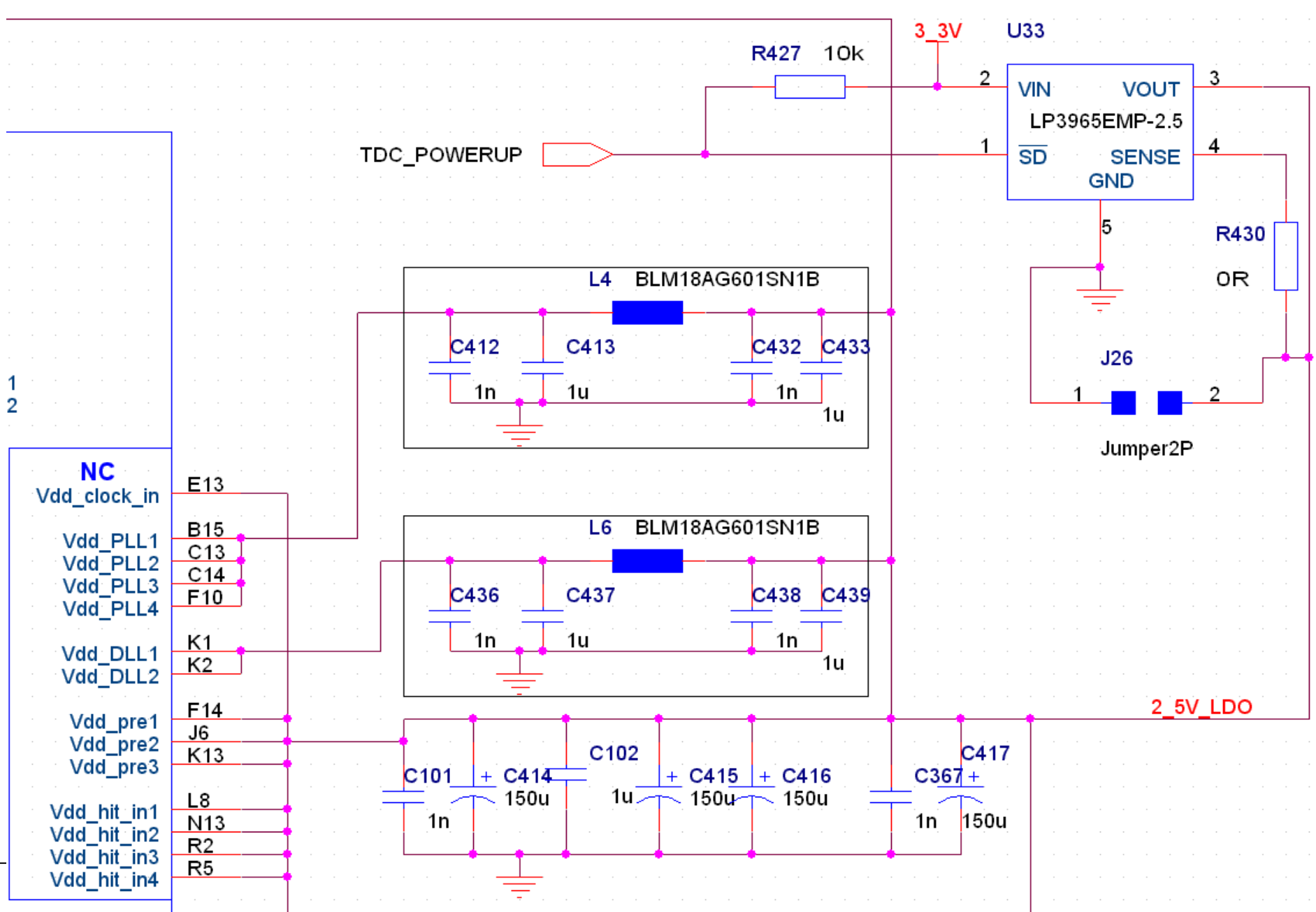

HADESTRB1
GSI - Darmstadt
14.01.05 MK/MT/PS
MARCIN KAJETANOWICZ
J21
TDC C
J22
TDC D
J23
J16
J17
J20
TDC B
J19
TDC A
J10
J18
J24
J25
SV OUT
CLOCK
FIFO empty
FIFO full
ETRAX
AXIS
ETRAX 100LX MCM 4+16
22545 E2
0441
TAIWAN
SWITCH1
SWITCH2
RESET
GND
48V DC
HPTDC 13
CERN Sep. 2004
TEST ERROR

TRB Module and components

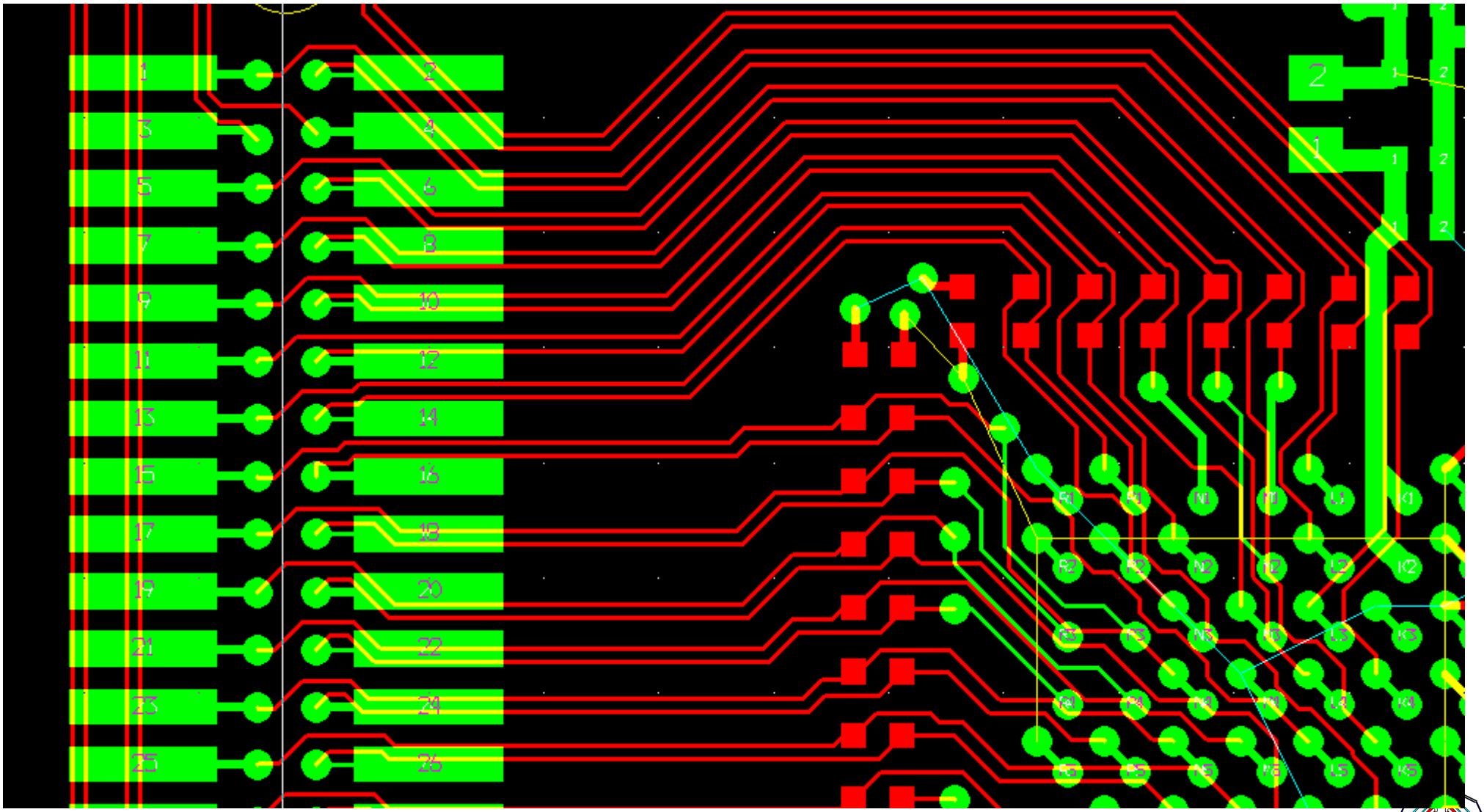


- 4*32 channels TDC, HPTDC
- 80 pin twisted pair cable, KEL connector
- Single Chip Computer with Ethernet
- FPGA
- DC/DC 48V, isolated
- Memory

Design Issues I

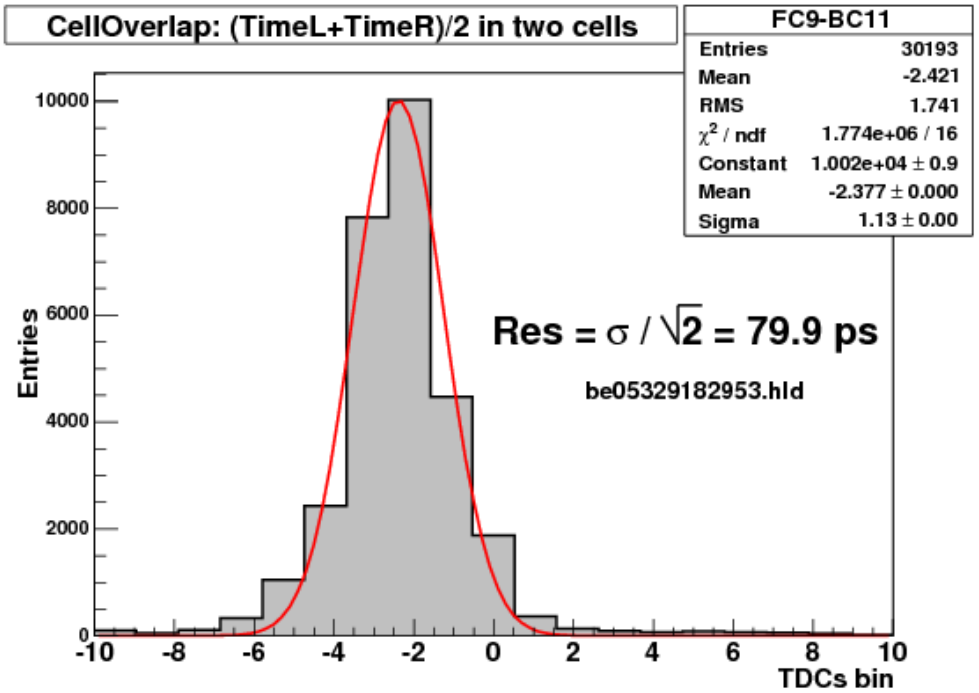


Design Issues II



Results I [1]

- Project of a larger team, very complex, time-consuming
- Concept is accepted and working: RPC Test Nov 05

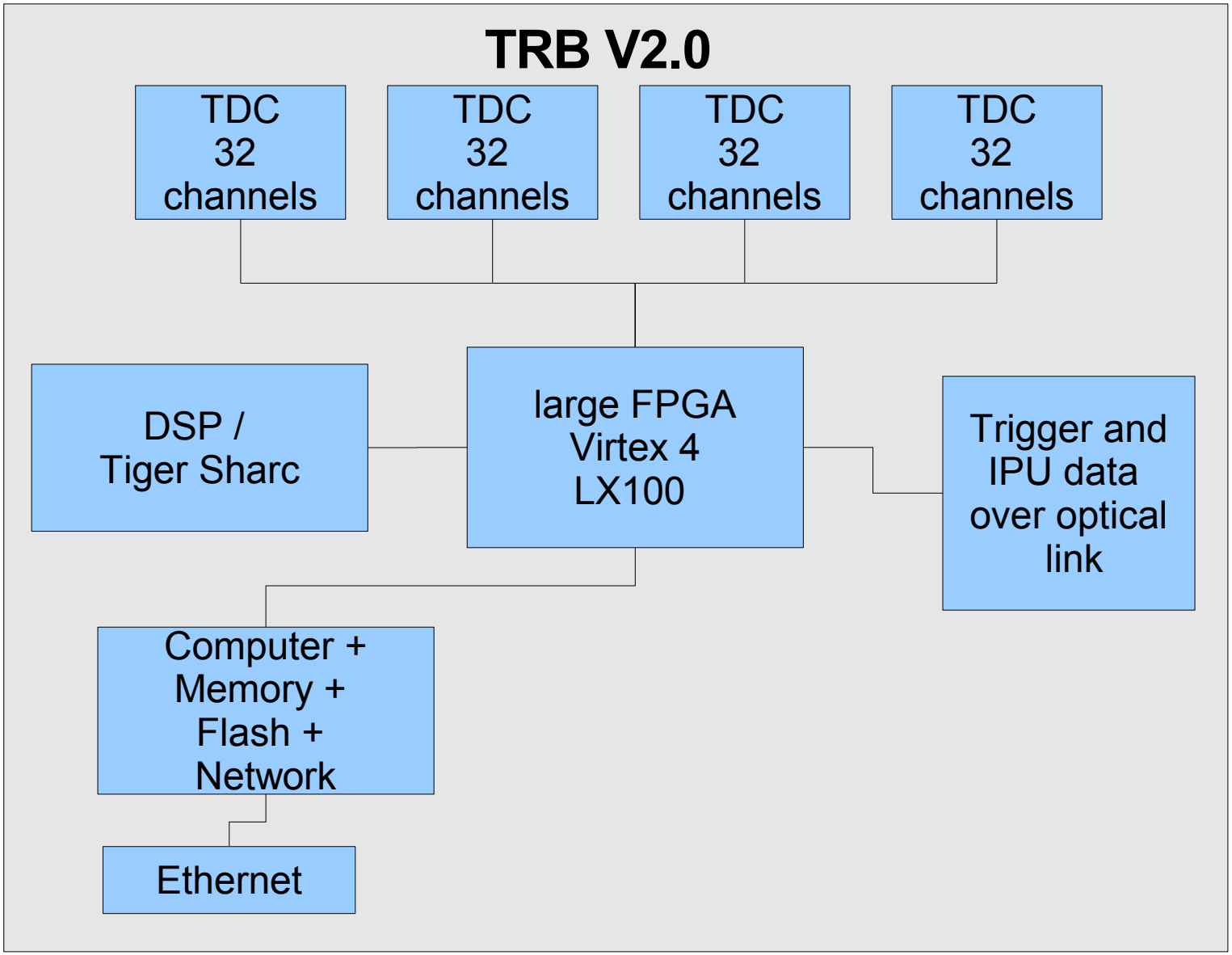


[1] M. Traxler , D. Gil, M. Kajetanowicz, K. Korcyl, M. Palka, P. Salabura, P. Skott, R. Trebacz: GSI Report 2006

Results II

- **Performance:**
  - sigma between 2 channels (4 TDCs): 38ps
  - LVL1 readout of 60 TDC-words/event: 35kHz
  - LVL2 readout of 60 words/event: 5-6kHz
  - LVL2 readout of empty events: 18-19kHz
  - all without DMA, no optimization in FPGA
- **TDC-Resolution**
  - sigma between 2 channels (4 TDCs): 38ps
  - no signs of crosstalk on TRB (has to be verified with more careful measurement)
  - RPC-detector channel resolution: 80ps

Future: TRB V2

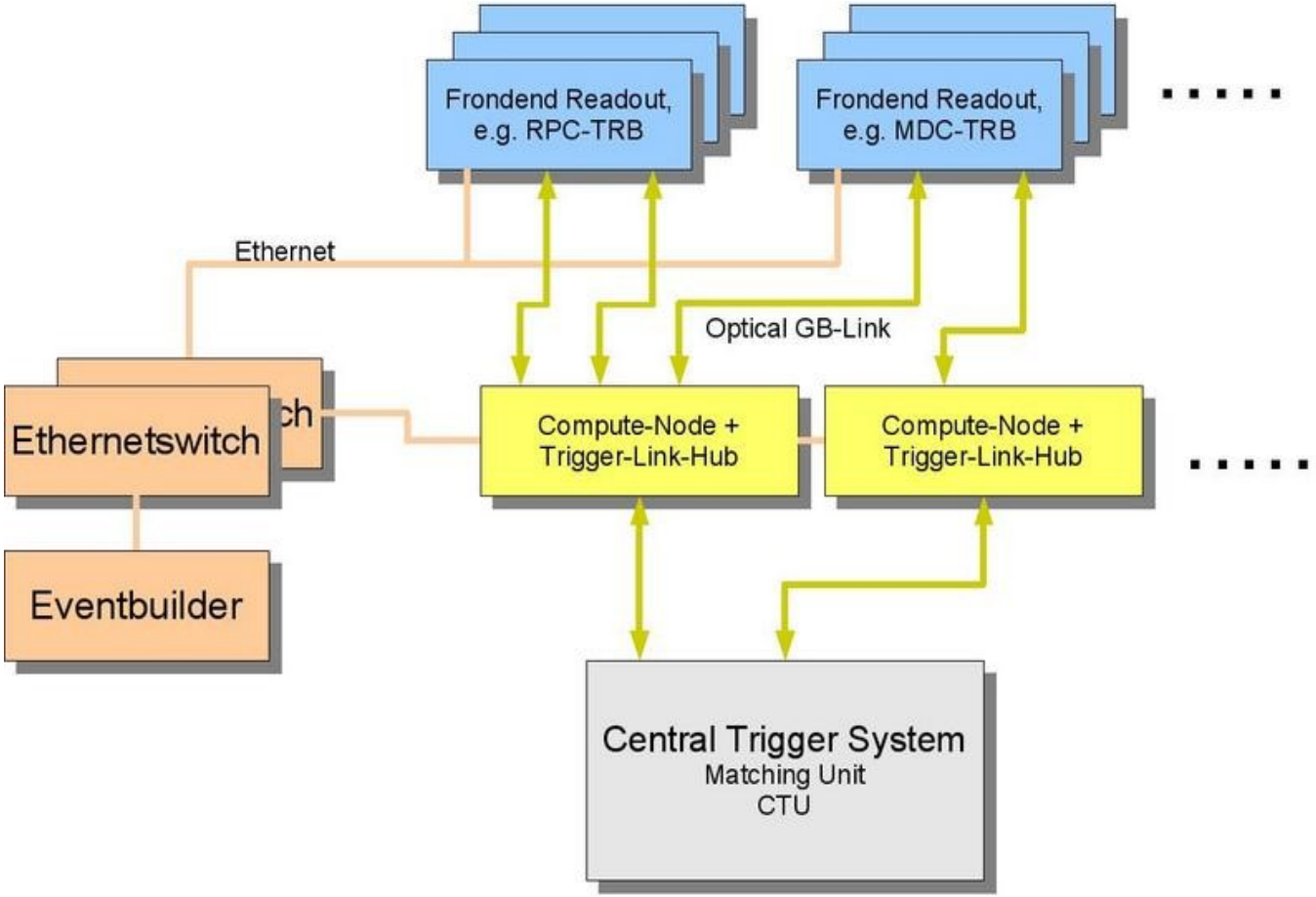


Future II

- Additional Features:
  - 2 Gbit optical link for online pattern-recognition data transfer **and** LVL1 and LVL2 trigger information (not timing)
  - 3 times faster CPU (21€/piece)
  - Large FPGA for online pattern-recognition, zero suppression....
  - DSP: Tiger-Sharc (TOF-algorithm)
  - option: remove TDCs, connectors for readout of:
    - MDC, RICH
  - Clock-Distribution and Power-Sequence Chips: Lattice

Appendix

- New Trigger Distribution and IPU-Data transport
  - http://hades-wiki.gsi.de/cgi-bin/view/DaqSlowControl/DaqUpgradeOverview
  - http://hades-wiki.gsi.de/cgi-bin/view/DaqSlowControl/NewTriggerBusNetwork



Summary

- **Things to learn from HADES-experiences:**
  - Don't allow a zoo of digital-hardware for every subsystem
  - Data transport issues are at least 10 times more demanding/time-consuming than the algorithm to implement (maybe connected to the zoo of hardware)
  - Think more about Low-Voltage Power-Distribution