Statusbericht GRISU

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EE-Gruppenmeeting

GSI Darmstadt

9. Februar 2009

weitere Vorträge

Verweis auf weitere GRISU Vorträge:

- IT/EE-Palaver (20.1.09):
  Untersuchung von Strahlungseffekten in anwendungs-spezifischen integrierten Schaltungen (ASIC) Strahlungseffekte
- CBM-XYTER Family Planing Workshop (5.12.2008)
  UMC 0.18µm radiation hardness studies
- EE-Gruppenmeeting (7.7.2008)
  GRISU Statusreport

via EE-Wiki → Projekte → GRISU

SEE Tests

SEE Tests mit Schwerionen an der GSI:

- X6 Bestrahlplatz
- 11,4 MeV/u
- 6 durchgeführte Bestrahlungstests
  - C-12 (3x)
  - Ar-40
  - Ni-58
  - Xe-132
- LET im Bereich von 1...62 MeV·cm²/mg (SiO_2)
  ➔ Q = 8..1300 fC

LET Messbereichsübersicht

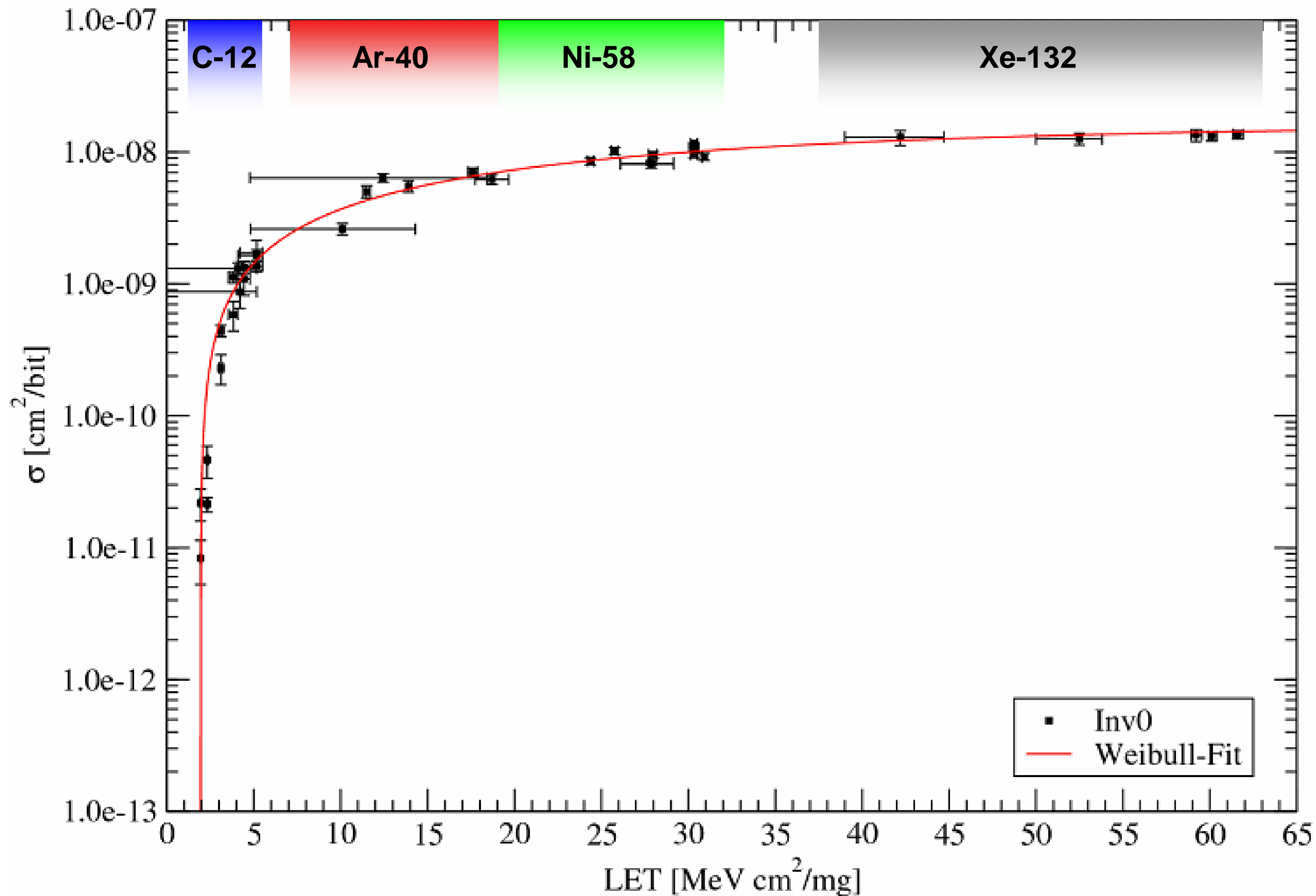
Übersicht der LET Bereiche der unter-schiedlichen Bestrahlungs-tests

Xe-132 - IC-FR 005
Ni-58 - IC-FR 005
Ar-40 - IC-FR 005
C-12 - IC-FR 005

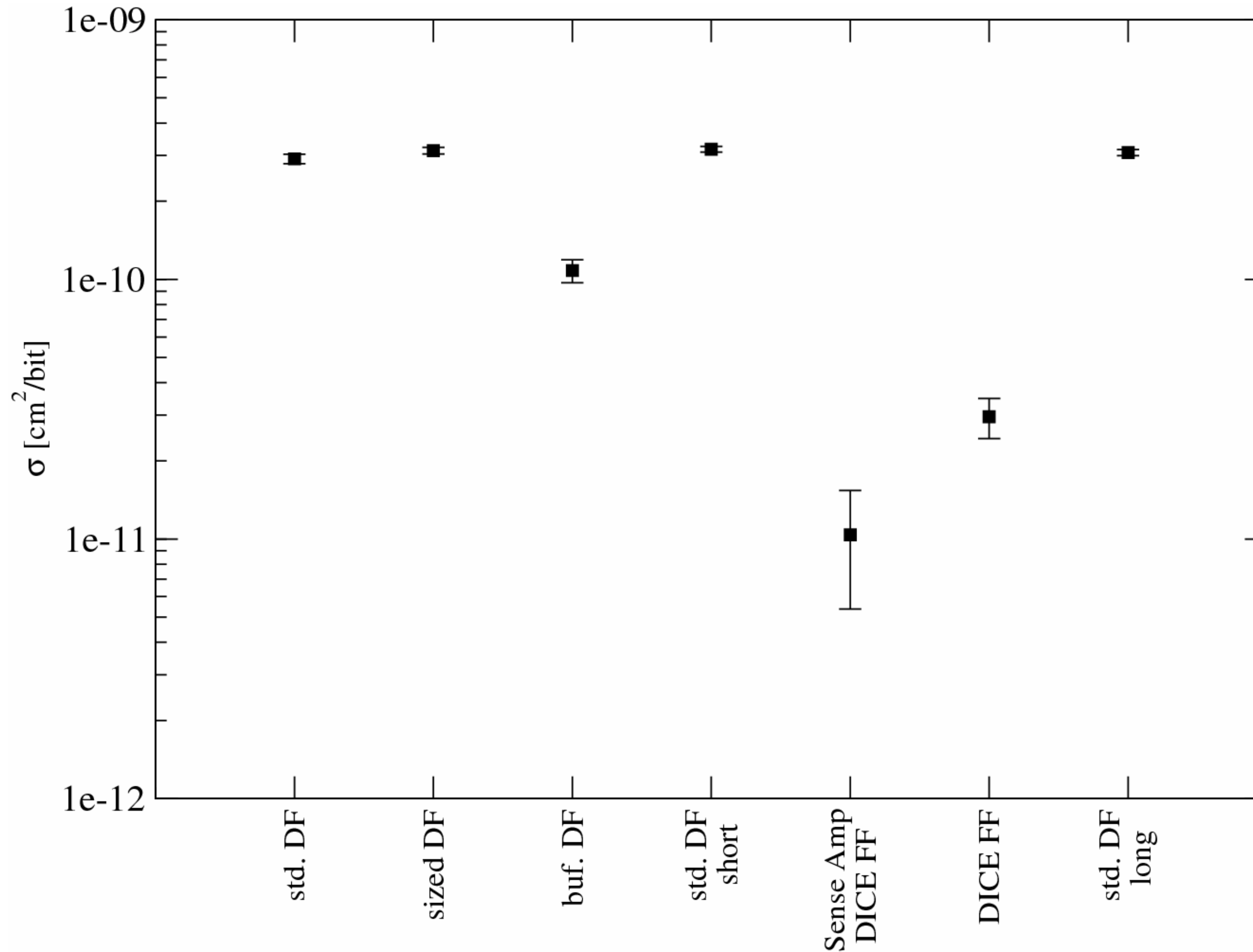
LET [MeV cm^2/mg]

Distance from exit window [cm]

Wirkungsquerschnitt (Inv.)



Wirkungsquerschnitt (DF)



Dual Interlock Cell (DICE)

DICE (Dual Interlock Cell) memory technologies are (more or less) immune against SEU flips.

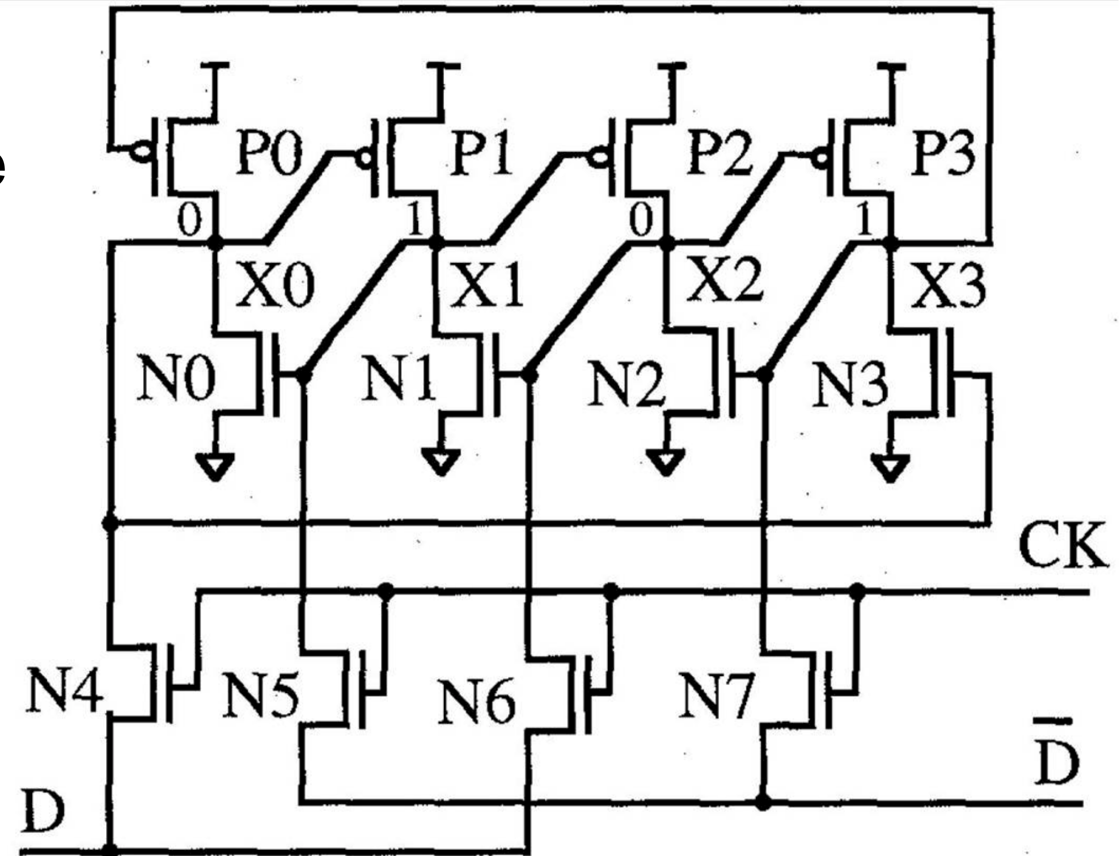
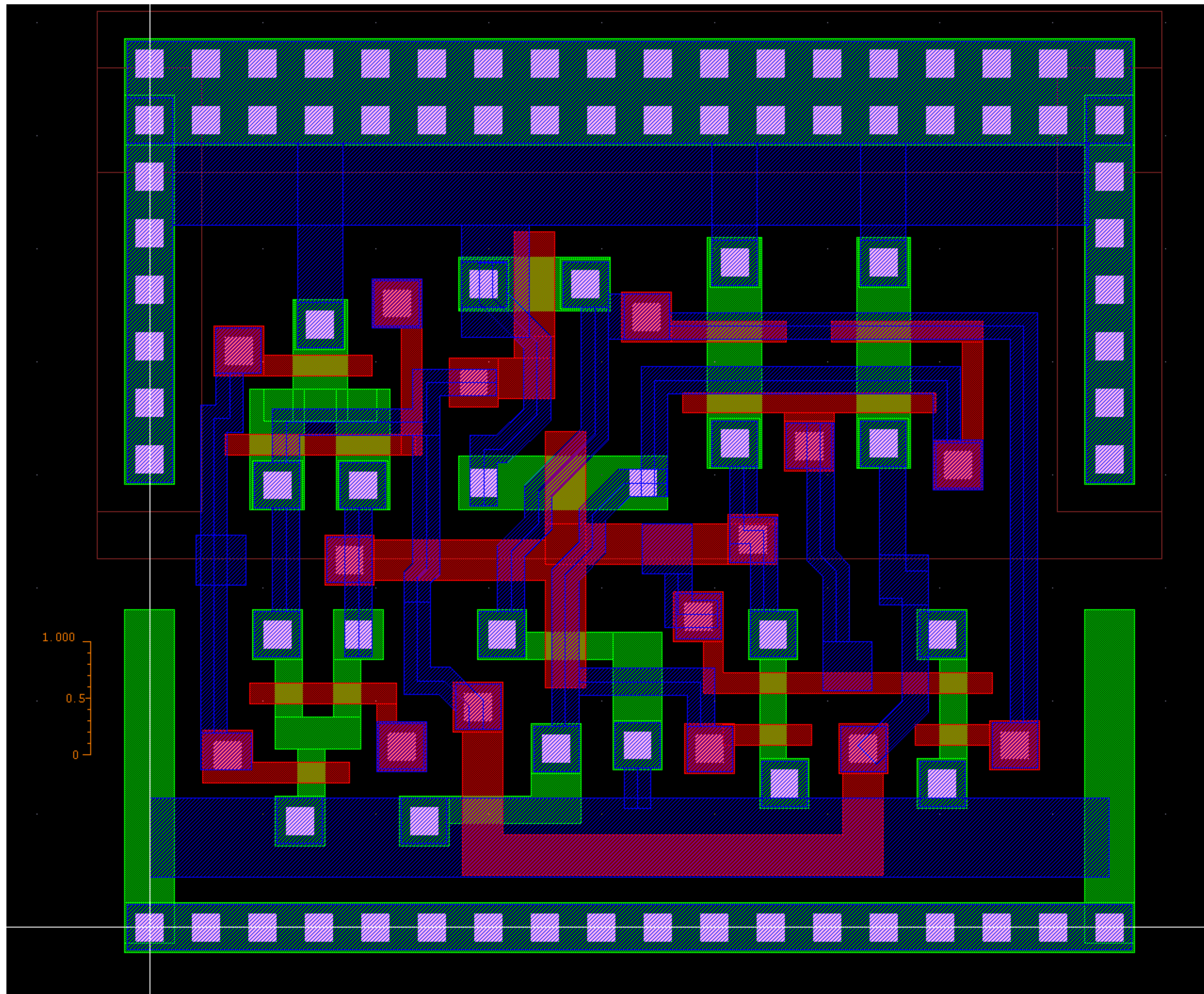


Fig. 4. The DICE Memory Cell

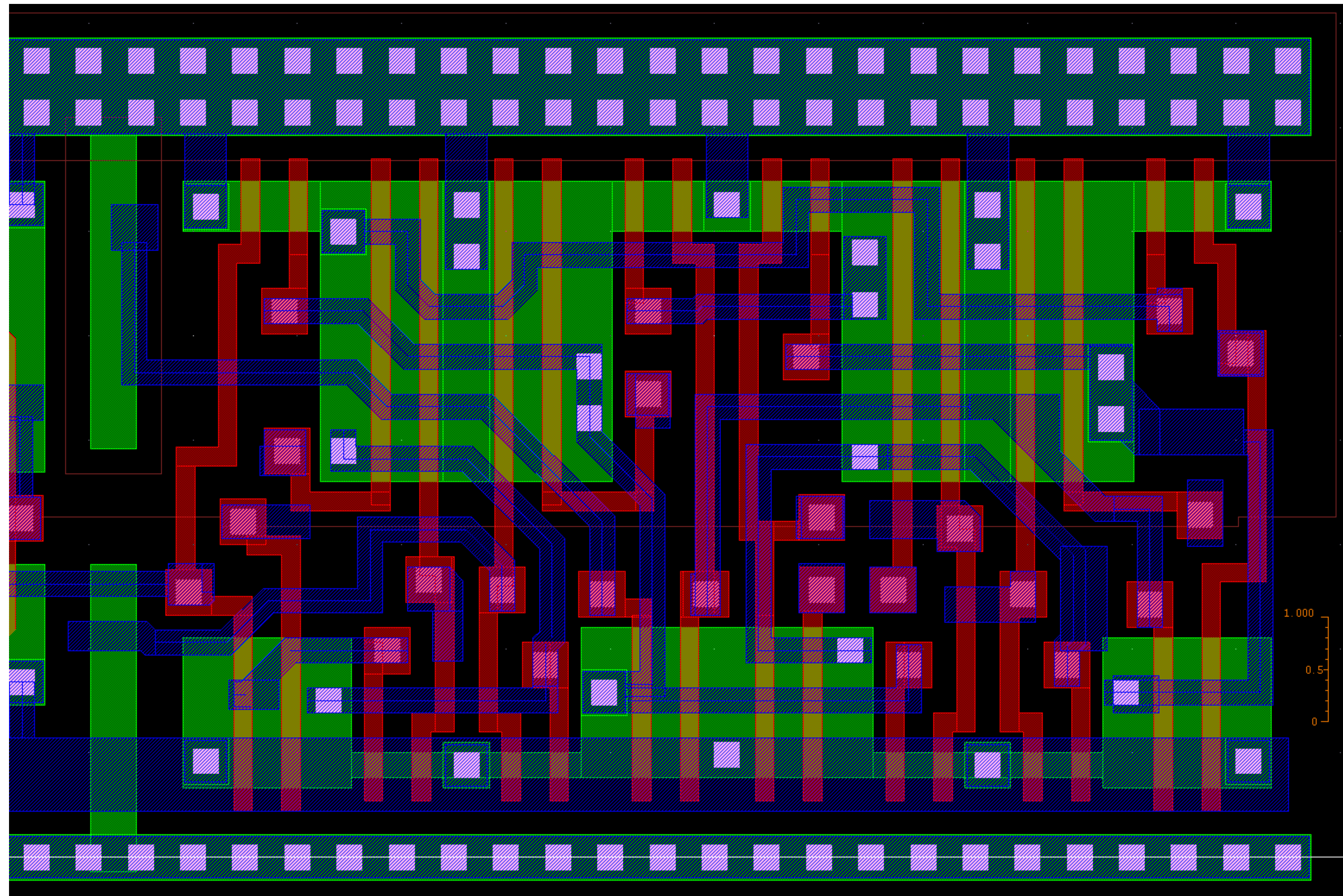
Reference:

T. Calin, M. Nicolaidis, R. Velazco
Upset Hardened Memory Design for Submicron CMOS Technology
IEEE Transactions on Nuclear Science, Vol. 43, No. 6, December 1996

Layout DICE Latch



Layout Sense Amp. DICE FF



SEE - Zusammenfassung

Zusammenfassung:

- erfolgreiche Durchführung von 6 Bestrahlungstests mit unterschiedlichen Schwerionen
- Ionisationskammer:
  - Auslese mit QFW Chip und aktiven Stromteiler
  - Anbindung des QFW an das FPGA-Board

Noch nicht verstanden:

- Warum die beiden DICE-Zellen nicht so SEU immun sind

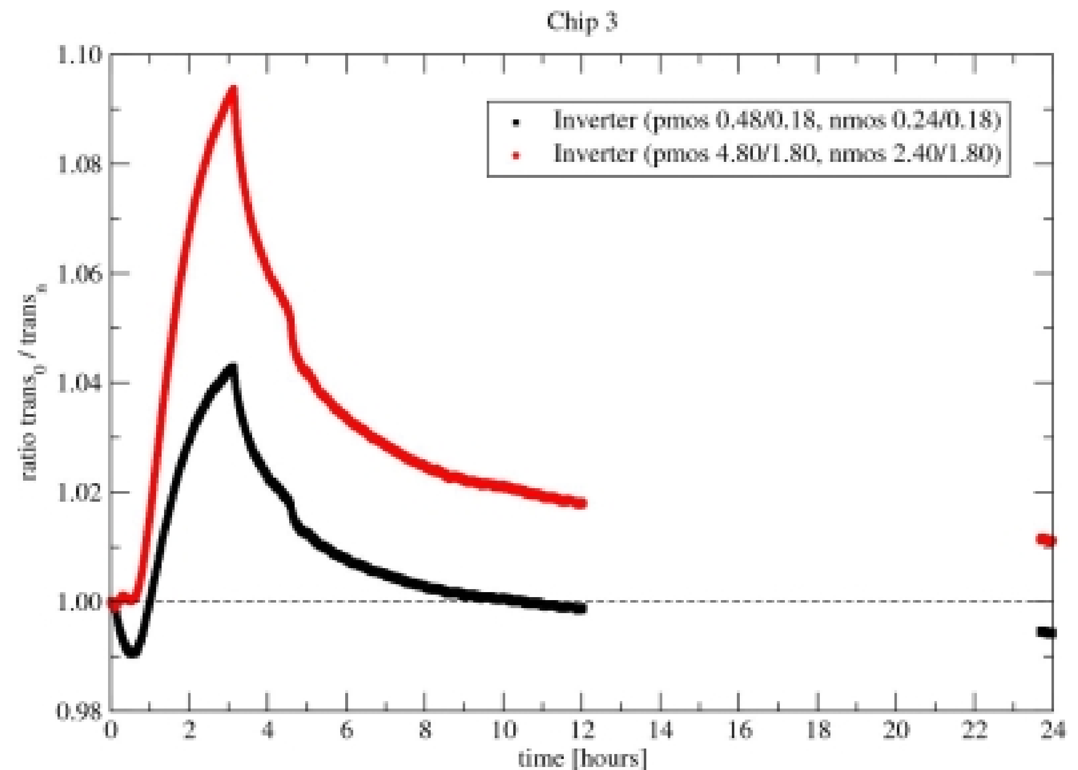
TID-Test am FZK

- 9 GRISU Chips bestrahlt
- Gesamtdosis je Chip zwischen 800krad and 2500krad(SiO_2)
- Dosisrate zwischen 200krad/h und 580krad/h
- Bestrahlungsmodi
  - Messung der Teststrukturen
    - Leckströme (online)
    - Schwellenspannung (offline)
    - Kennlinien (offline)
  - Messung des Gesamtverhaltens des GRISU-Testchips
    - Frequenz des Ringoszillators (online)
    - Stromaufnahme (online)

TID tests – complete chip

Measurement of two ring oscillators on GRISU 2 test chip

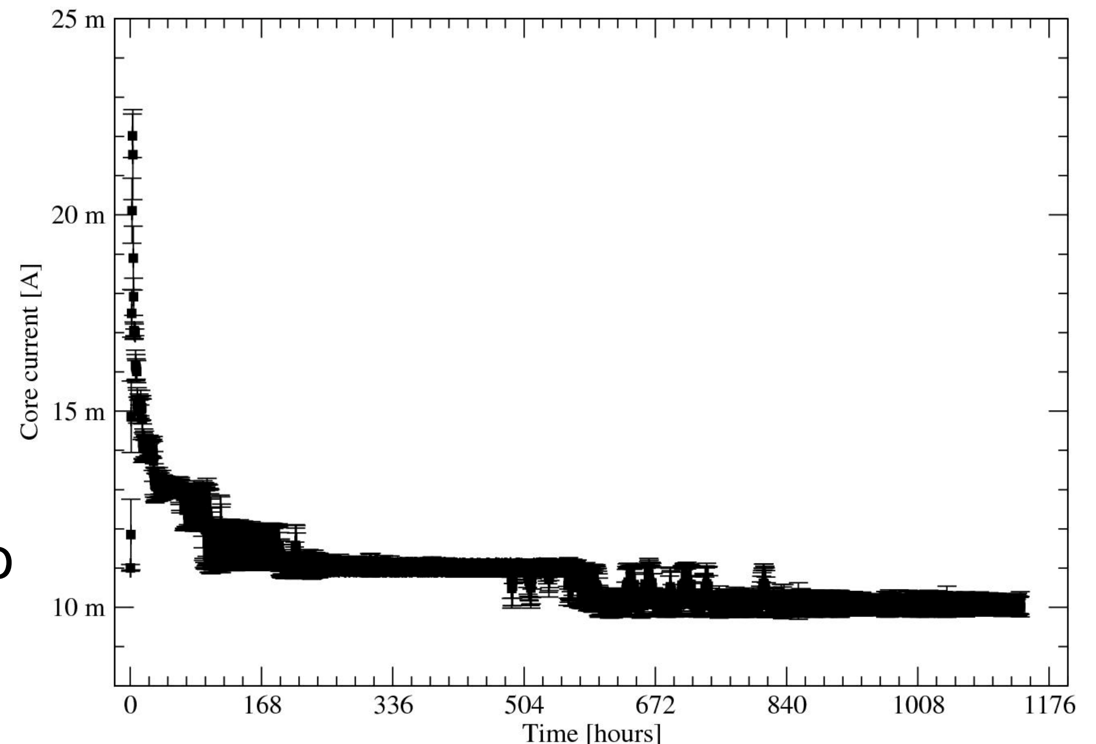
- Total dose: 1.5Mrad
  - at 490krad/h
- Decrease of the transit time
  - ~ 4% for minimum size inv.
  - ~ 10% for up-sized inv.
- Good annealing at room temperature
  - for min. size: even faster
- Up to 250krad:
  - min. size inverter gets faster
  - up-sized inverter keeps stable



TID tests – complete chip

Measurement of power consumption on GRISU 2 test chip (core)

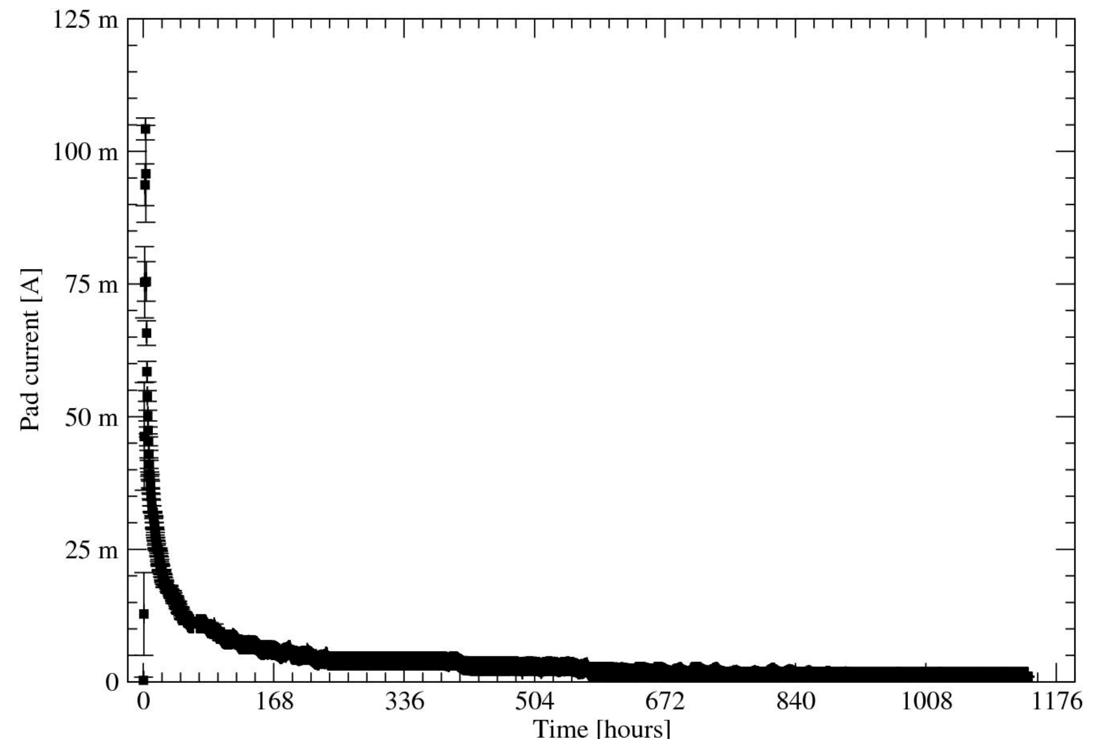
- Total dose: 1.5Mrad
  - at 490krad/h
- Increase of the core power consumption
  - from 10mA (pre-rad) to 22mA (1.5Mrad)
- Annealing at room temp.
  - power consumption back to pre-radiated value after 6 weeks



TID tests – complete chip

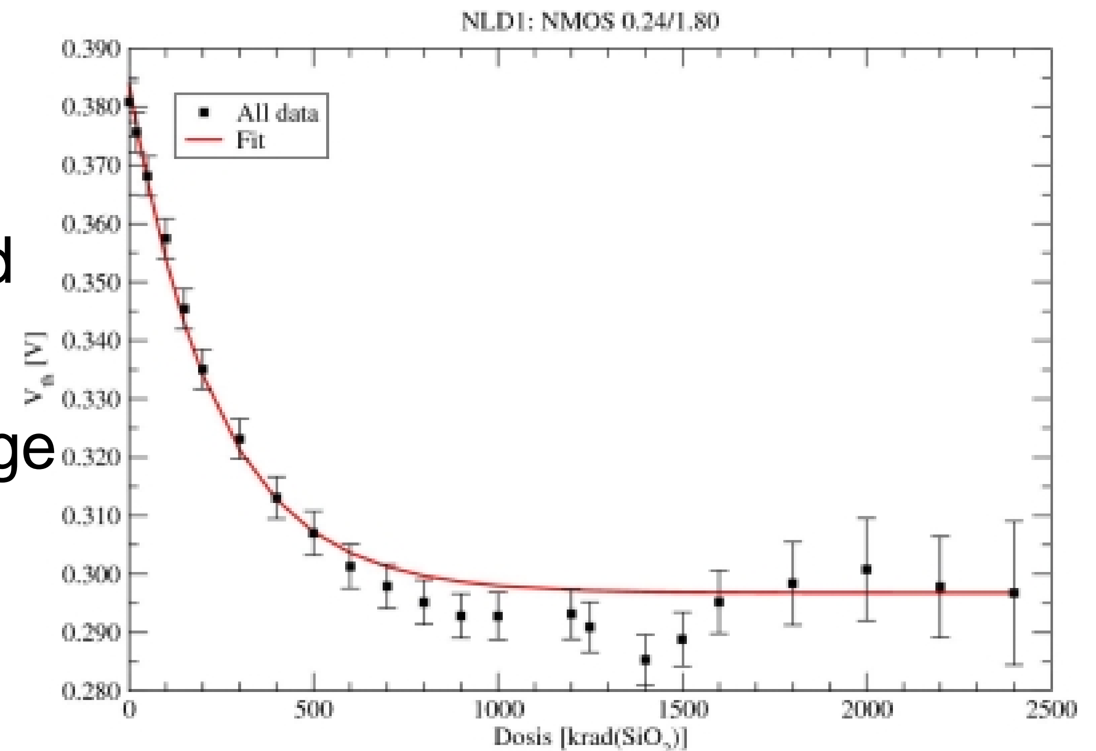
Measurement of power consumption on GRISU 2 test chip (pad)

- Total dose: 1.5Mrad
  - at 490krad/h
- Increase of the pad power consumption
  - from 1mA (pre-rad) to 105mA (1.5Mrad)
- Annealing at room temp.
  - power consumption also back to pre-radiated value after 6 weeks



TID tests – single transistors

Measurements of the transistor characteristics and calculation of the threshold voltages for different dose levels
(e.g. NMOS 0.24/1.80)

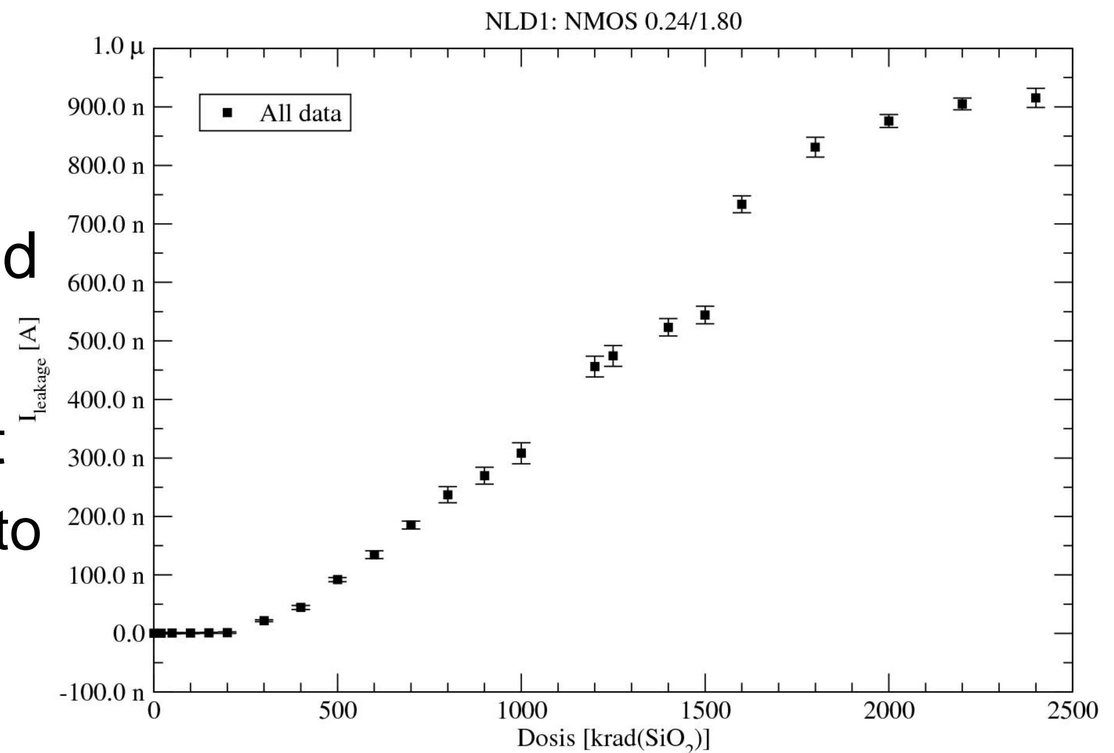


- In total 6 chips are irradiated
- Total dose up to 2.5Mrad
- Decrease of threshold voltage
  - ~ 20% after 1Mrd
  - no further change after 1Mrad

TID tests – single transistors

Measurements of the transistor characteristics and extraction of the leakage current for different dose levels (e.g. NMOS 0.24/1.80)

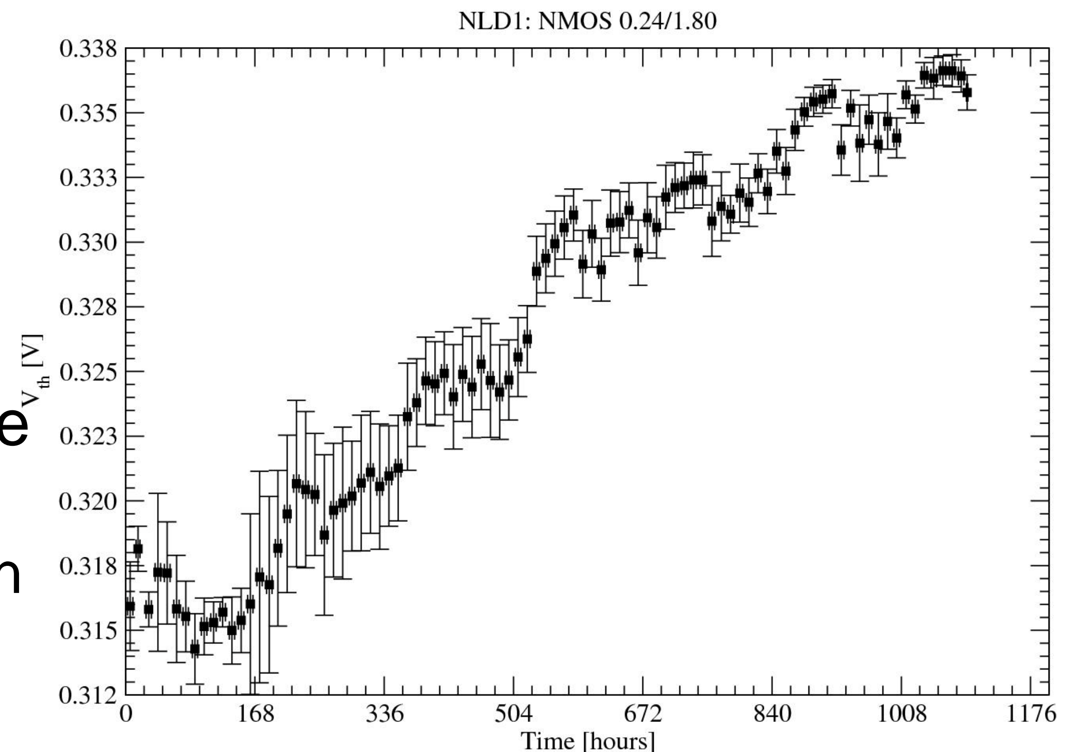
- In total 6 chips are irradiated
- Total dose up to 2.5Mrad
- Increase of leakage current
  - no significant increase up to 200krad
  - by 3 orders of magnitude after 2.5Mrad



TID tests – single transistors

Measurements of the annealing and calculation of the threshold voltage for different dose levels (e.g. NMOS 0.24/1.80)

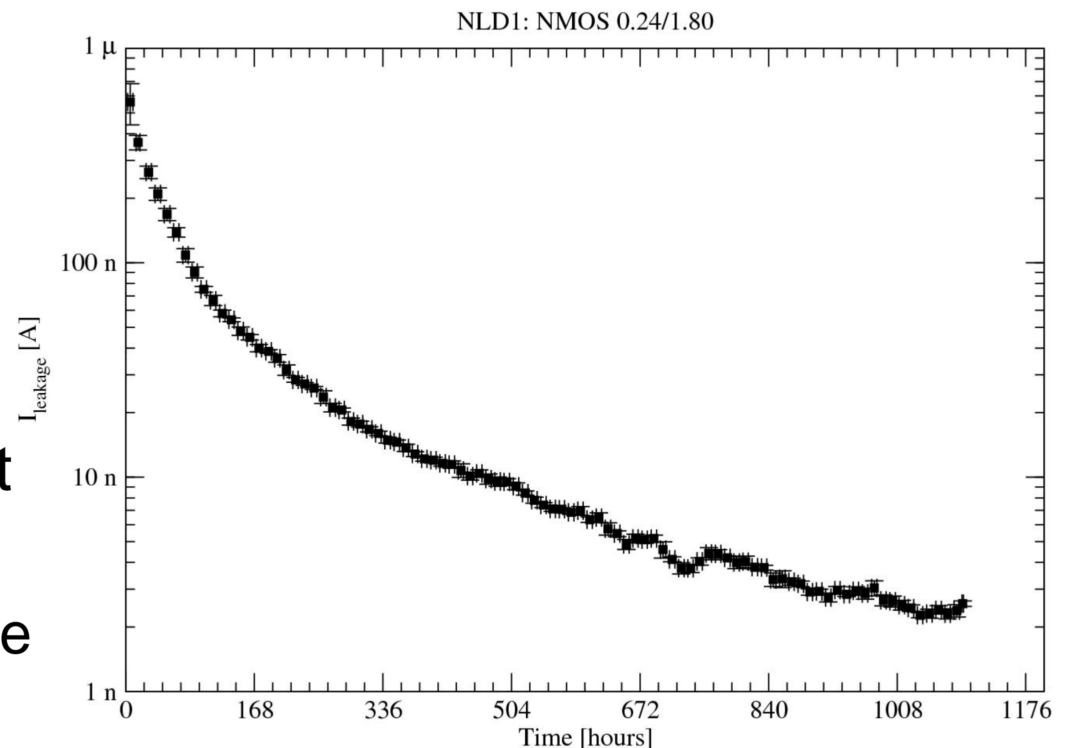
- Detailed annealing scans only with one 1 chip
- 2.5Mrad total dose
- Annealing at room temp.
- Increase of threshold voltage after 6 weeks
  - still 10% under pre-radiation value
  - but no saturation reached (maybe further increase possible)



TID tests – single transistors

Measurements of the annealing and extraction of the leakage current for different dose levels (e.g. NMOS 0.24/1.80)

- Detailed annealing scans only with one 1 chip
- 2.5Mrad total dose
- Annealing at room temp.
- Decrease of leakage current after 6 weeks
  - almost back to pre-rad value



TID summary

- Final analyse of measured data
- UMC process shows good annealing at room temperature (at least at high dose rates)
  - maybe a second irradiation campaign with low dose rates
  - long term test with a gamma source
- Simulation models slightly differs from measured characteristics (especially between small and large Ugs)
- Not shown:
  - Offset current for zero-Vth transistors are much higher than predicted from simulation
  - measured transition time for minimum size inverters differs ~40% from simulation
- ...