iRoC Technologies – The Soft Error Solution

Answers to Frequently Asked Questions Regarding iRoC's Testing Methodology For SRAM-based FPGAs

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Q. What does iRoC do?

A. iRoC Technologies develops and licenses soft error design solutions and test services to enhance the security, quality and reliability of nanometer integrated circuits

Test Description & Results

Q. Actel released a report April 19 indicating that normal neutron flux even at the Earth's surface can alter the configuration of SRAM-based FPGAs. Actel claims that its antifuse and flash-based field-programmable gate arrays are a better choice than SRAM-based parts in failure-sensitive applications. Does iRoC agree with this assertion?

A. Within our SERTEST™ database that encompasses a bit less than 100 different DUTs and more than 1000 different test conditions, we have clearly observed the highest SER in SRAM with a worsened situation using nanometer technologies. At the same time, flash memories are by far one of the least sensitive to SEU. As a result, the report issued by Actel is consistent with our database.

Q. How was the test conducted?

A. Actel contracted with iRoC, a specialist in single-event-upset testing, simulating and protection, to test different types of FPGA devices. The choice of using iRoC, an independent lab with a strong radiation test track record, assured results conforming to the highest quality standards. Using the SERTEST shuttle, the tests were performed at the Los Alamos facility. This beam is very consistent with the terrestrial neutron spectrum.

The tests were performed on 0.22-micron flash and 0.15-micron antifuse devices from Actel, and on 0.13-micron Altera and 90-nanometer Xilinx Spartan SRAM FPGAs. iROC adopted the procedure defined in the JESD-89 standard for the tests. The standard describes both a procedure for accelerated life testing for neutron radiation and one for estimating actual failure-in-time (FIT) rates at normal atmospheric radiation levels from the measured results.

Q. How do these errors occur?

A. Coming from the outer space, heavy ions are continuously bombarding the earth that is protected by a magnetic field. However, some ions are penetrating the atmosphere and through multiple atom collisions, these ions are generating neutrons that reach earth ground level. This neutron flux is increasing with altitude and depends also on latitude. By itself, a neutron is painless, but when a neutron collides a silicon atom it can create 132 different ions with various energies that can generate transient currents in a transistor. This current can cause changes in the SRAM bits that configure the logic cells and interconnect matrices of FPGAs, potentially causing errors in the behavior of the system.

The failure rate per bit cell is usually pretty small. However, using a large amount of bits or devices in large electronic systems designs can reach the threshold where errors occur in a visible timeframe, on the order of some months or weeks. The consequence of such errors in an SRAM-based FPGA is potentially more damageable than in a SoC since the application programmed could be lost with some necessary latency to recover.

Q. What were the results?

A. The radiation test performed at LANSCE had a goal to compare Soft Error sensitivity for different technologies and providers of FPGA. Using exactly the same test conditions and the same test environment, the tested devices could have been compared and benchmarked with a consistent methodology. Three types of FPGAs have been tested: SRAM-based, Flash-based and antifuse-based FPGA.

The SRAM-based devices did show significantly more upsets, and more changes to their operation, than did the flash based parts. The behavior of the SRAM-based FPGAs was essentially consistent with the behavior of other SRAM devices we have tested, using the same process nodes.

Specifically, over the course of the radiation dose, the nominally 1 million-gate Altera EP1C20 exhibited 453 functional failures. The nominally 1 million-gate Xilinx XC3S1000 exhibited 1,936 configuration-cell upsets and 405 functional errors, and the nominally 3 million-gate Xilinx XC2V3000 showed 3,459 configuration upsets and 349 functional errors. Neither the antifuse Actel AX1000 nor the flash APA1000 displayed any functional errors.

Configuration data was not checked on the Actel parts because it was not readily available. Nor was it checked on the Altera part, because the experimenters were unable to get the configuration read-back function to work until after the experiment.

Using the formulas in JESD-89, the data predicted that at sea level the Altera device would experience 460 FIT and the two Xilinx devices 320 and 1,150 FIT respectively. A failure in time is one failure in a billion hours — about 114,000 years.

The report is available at www.actel.com/documents/OverveiwRadResultsIROC.pdf

Q. Why there is such a big difference between the FIT measured for the two Xilinx FPGAs?

A. The cosmic-ray sensitivities of the two Xilinx FPGA are indeed very similar. In the report (doc ref RE_2_ACTEL_SERTEST_DEC_03_ENG_TR_006) in table 27 page 39, the FIT ratio of XC2V3000 (Virtex-II) and XC3S1000 (Spartan-3) is 3.6. This is because FIT units in the report are "FIT per Device," the choice agreed to for the test. The XC2V3000 size is 3 times larger than XC3S1000, the XC2V3000 has 9.5 Mbits of configuration memory and the XC3S1000 has 3.2 Mbits of configuration memory. Therefore, if the FIT were presented in units of "FIT per bit of configuration memory" both FIT numbers would be very similar.

Q. What is the soft error trend over the industry today?

A. iRoC has been tested more than 100 different devices using more than 1,000 test conditions. Along these tests, iRoC has observed a clear degradation of reliability in devices using nanometer technologies. SRAM are by far the most sensitive memories reaching the 2,000 FIT/Mb in certain conditions with the 90nm process. However, these results are very dependant on in-the-field parameters such as voltage used, temperature and frequency. Flash memories have shown a very low SER, either to neutron or to heavy ions.

Q. What is the soft error pain for the end customer?

A. A soft error is becoming a major contributor to the growing number of errors in-the-field. These soft errors are creating a wrong bit inside the system. Depending on how and when the bit is used, the system can either crash, requiring a reboot, or, more insidiously deliver wrong information that can corrupt a whole chain of systems. No communication protocols are efficient since the error occurred into the silicon by itself. At the end of the day, the OEM would potentially increase its maintenance and availability costs, and lose market share. Since no specific mechanisms are embedded into chips or systems to track this type of errors, it’s still difficult to provide a realistic ratio on error in-the-field implications in system crashes versus software bugs or power disruption.

Regarding Altera's and Xilinx's Response

Q. SRAM FPGA vendors like Xilinx and Altera are saying that the new data is consistent with a large body of existing measurements that in fact show how resistant SRAM-based FPGAs are to neutron radiation.

A. Through our large test data base, iRoC doesn't see any enhancement of SER neutrons of devices. If the increase of SER between a 0.25um and 90nm process could be interpreted not to be exponential, it is clearly linearly more significant. These results are also confirmed through 3D simulation done by our physic experts. Basically, there is no difference between SRAM technologies utilized for FPGA and standalone SRAM or embedded SRAM tested by iRoC along its SERTEST shuttle, and this current report is very consistent with our previous test experience. iRoC is not providing any judgment about the "resistance" of a device that is more on the end customer or OEM side, but iRoC provides a FIT metric standardized by an international committee, JEDEC.

Q. Vendors of the SRAM-based devices seem to agree that flash- and antifuse-based FPGAs are more resistant to radiation-induced upset of their configurations. But they claim that there is no significant issue (i.e. reliability impact) outside the space market. How do you interpret the implications of the results at sea level?

A. For certain sea-level application OEMs have set the SER FIT rate as a key specification to be matched. This is driven by two trends:

- The SER FIT per cell is increasing with respect of the technology node used

- The number of bits and number of devices used per system is increasing as well.

iRoC is already working with key OEM in mainstream market for networking equipment, telecom equipment, smartcard industry and transportation industry. Most of iRoC customers advocate that SER is becoming a concern because it falls into the non determinist world of electronic systems and can affect directly their business and market shares.

Q. Do you think the solution strategies of triple redundancy, error-correcting or parity codes and redundancy in time are the answer?

A. Most of solutions known today are well suited for space applications or for application where silicon cost is not a constraint. Technically wise, these solutions work perfectly well. But these solutions bring various penalties that can jeopardize a whole device business: ECC brings area cost but beyond that, adds also performance penalty, TMR is barely affordable for most of mainstream application. Used as is, these solutions will throw nanometer process business advantages far behind the previous process node. iRoC strongly believes soft error SoC solution resides in the awareness and the use of a SER design flow by designers. The solution is more in how and when to use these techniques than hardening everything blindly. Therefore, iRoC is developing a body of expertise from testing, simulating and designing soft error products.

<u>The Future</u>

Q. Does iRoC believe the number of upset occurrences will only get worse as geometries get finer? Why?

A. Prediction of SER in future technologies has been the mainstay activity of SER experts for many years. Using advanced T-CAD tools performing first 2D and then, since the late 90's, 3D device simulation, experts have been able to identify what are the key parameters involved in neutron and alpha particle reaction with silicon. Besides these simulations, a lot of experiments have been conducted under radiation to calibrate and validate simulations. All data available today indicate that there has been a sustained increase of upset occurrences as the process node shrunk up to the 130nm node. To mitigate this effect, one significant step has been done with Boron10 removal (BPSG) during the process; then, one can expect a stabilization of upsets per bit cell.

To get a qualitative idea of upset occurrence trends in future technology, for example in SRAM nodes, the first step is to consider the two main parameters influencing the SEU sensitivity: the critical charge (Qc) and the sensitive volume of the cell. The lower is Qc, the higher sensitive is the cell. But the smaller the sensitive volume, the less probable is a neutron collision with a silicon atom. From our internal simulation and other different sources, such as NEC Corporation (Hane and all, IEEE SISPAD 2003), these two effects are competing pretty much in the same range, so that the upset occurrences per bit cell could be expected to be the same along process node shrinking.

At the same time, in nanometer design, the transistor density is higher and SEU sensitive volumes are closer leading to two results:

- The global sensitive volume per die is larger and neutron collision probability is increasing
- Transistors are becoming so close that higher multiple bit upsets are observed and are more damageable in applications since standard ECC cannot detect and correct this type of MBU.