Blueprints NI_FPGA_PPG

Status: 12.11.2009

Requirements	Status	Comments
• 64 digital outputs for device triggering	ok	
• dt = 12.5ns • dt = 25ns	ok	FPGA clock at 80 MHz, PCI/PXI 7811 FPGA clock at 40 MHz, PCI/PXI 7813
• Lowest time for one pattern 800ns • Lowest time for one pattern 1600ns • Lowest time for one pattern 12.5ns • Lowest time for one pattern 25ns	ok	80MHz, if jump commands are used 40MHz, if jump commands are used 80MHz, if **no** jump commands are used 40MHz, if **no** jump commands are used
• 8 digital inputs for conditional execution (triggering) of the PPG [if trigger condition applied PPG continuous with next command execution], can be handled user-defined and more than once	ok	Constant delay (with jitter of one clock tick) between trigger edge and next command execution ~125ns (80MHz) or xxx ns (40MHz). Due to reading new data from FIFO and register handling of I/O pins.
• different pattern (command) sequences should be executable without reloading of the PPG	ok	end every command sequence with one stop-command and start desired sequence over memory address of first command belongs to the sequence
• PPG should be used as single device	ok	instrument drivers
• repeated execution of pattern sequences directly on the FPGA card	ok	realised by special jump-command which is defined by memory address for the back-jump and the number of iterations
• time scans	ok	changing of command time and/ or complete command is possible
• load card with configuration file	ok	
• continous (repeated) execution without external handling	ok	

Port assignment

– 64 digital outputs / 8 digital inputs

connector 0 --> digial outputs - lines 0-31
connector 0 --> digital inputs - lines 32-39
connector 1 --> digital outputs - lines 0-31
connector 1 --> digital outputs - line 39 (state indicator)

Memory depth = 4000 memory addresses → commands

Command handling in memory blocks

	mem0 (U8)	mem1 (U32)	mem2 (U32)	mem3 (U32)
$time	3	line 0-31, connector 0	line 0-31, connector 1	time value [ticks]
$wait	2			line 32-39, connector 1
$jump	1	control variable	number of iterations	Memory address
$stop	0	line 0-31, connector 0	line 0-31, connector 0	unused

Command specifications

$wait – time [in us] for FPGA clocked at 80MHz (PCI/PXI 7811)

- ✓ $t_{\_max}$ = 4294967295 ticks x 12.5 ns = 53 s
- ✓ $t_{\_min}$ = 0.800 us (if jump commands are used)
- ✓ $t_{\_min}$ = 0.0125 us (if no jump commands are used)
- ✓ dt = 12.5ns (with conversion to ticks values will be rounded to integer values U32!!!)

$wait – time [in us] for FPGA clocked at 40MHz (PCI/PXI 7813) have to be multiplied by a factor of two!!!

$jump – number of iterations

- ✓ i = 4294967295

File syntax

```
//
// Pattern Definition:
//--------------------------------------------------------------------------
//                time [us]       !state of digital outputs
//
$time           1               !0x0                                    //hexadecimal
$time           0,9             !0xFFFFFFFF00000000
$time           100             !0x
$time           500             !0xFFFFFFFF00000000
//--------------------------------------------------------------------------
//                memory address  iterations
$jump           0               x1000
//--------------------------------------------------------------------------
//                condition       !state of digital outputs
$wait           !0x             !0xFFFFFFFF00000000
//--------------------------------------------------------------------------
//                time [us]       !state of digital outputs
$time           100             !0x0
$time           500000          !0xFFFFFFFF00000000
$stop                           !0xFFFFFFFF00000000
```

More than one command sequences can be listed and loaded to the FPGA card. Every sequence have to be ended with a stop-command. Decision of executed sequence over memory address during start.

Command syntax in VIs NI_FPGA_PPG_load.vi / NI_FPGA_PPG_load_command.vi

cmd	example	syntax
$time	$time :: 1000 :: 123 :: 123	*cmd:: time value :: line 0-31, connector 0 :: line 0-31, connector 1*
$wait	$wait :: 2 :: 123 :: 123	*cmd :: condition, line 32-39, connector 1 :: line 0-31, connector0 :: line 0-31, connector 1*
$jump	$jump :: 0 :: 500 :: 500	*cmd :: address :: unused ::number of iterations*
$stop	$stop :: 0 :: 0 :: 0	*cmd :: unused :: line 0-31, connector 0 :: line 0-31, connector 1*

Notes:

- space characters are only for better clarification → DON'T USE!!!
- every command in NI_FPGA_PPG_load.vi must be in the form x::x::x::x !!! Also if some data [marked with unsed] are not required

Error codes

code	comment
-1073999999	resource not initialized (no commands and invalid mem address)
-1073999998	wrong memory address (address > Nof commands)
-1073999997	invalid time value (probably too short)
-1073999996	cannot start FPGA because one or more errors occured
-1073999995	FIFO (internal) empty unexpectedly
-1073999994	DMA FIFO (download from host) full unexpectedly
-1073999993-1073999981	unknown error 7-19
-1073999980	can't change state while pattern output is in progress