EE Digital Electronics:

Location:	doc\ vulom1\vulom_v6.doc
Date:	25.01.2007
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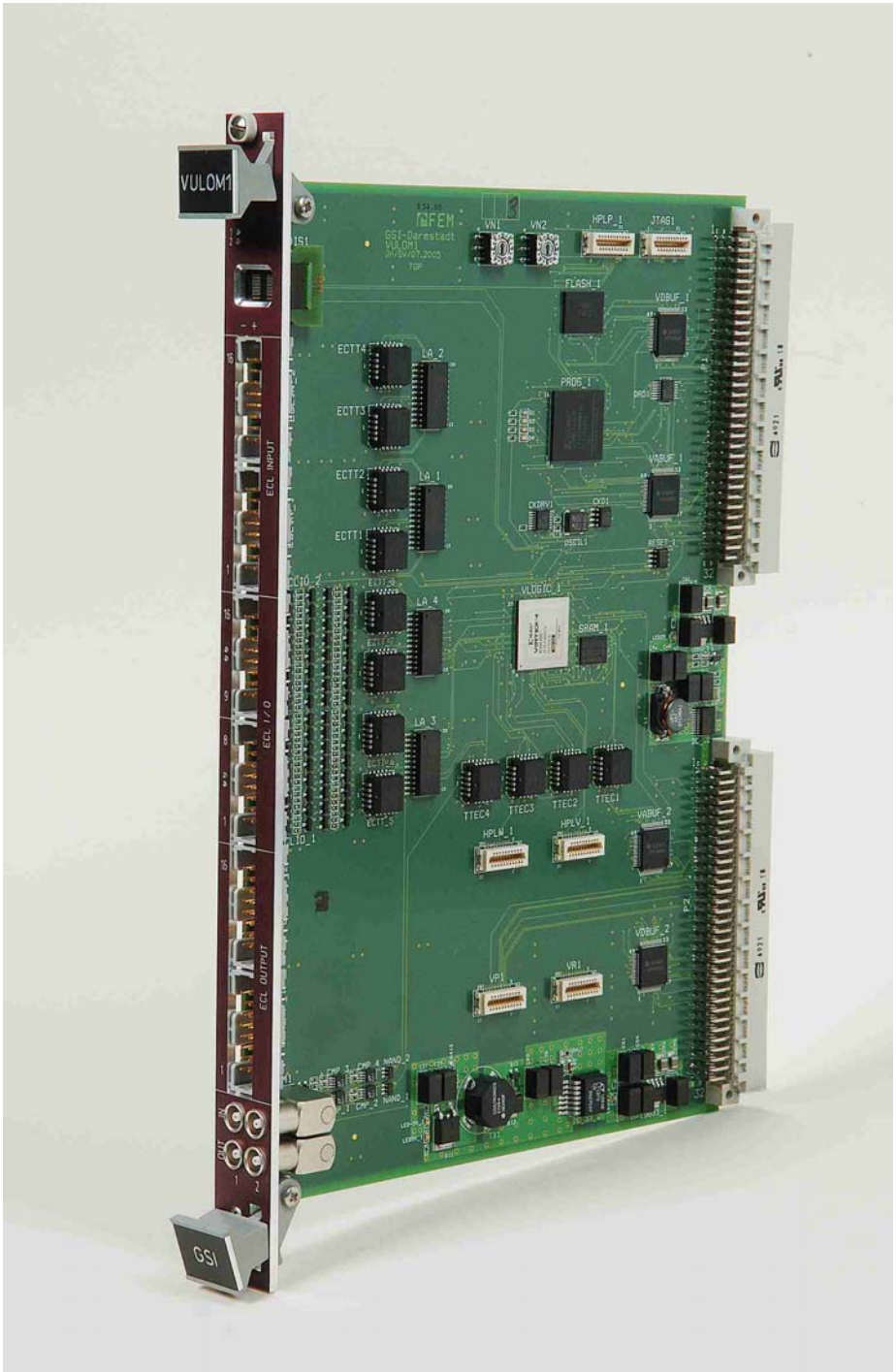
Title:	VULOM1, VME Universal Logic Module, Version 1



1.1 VME Logic Module Features

The VME Logic Module is equipped with VIRTEX 4 FPGA and ECL front panel inputs (up to 32) and outputs (up to 32). All functions of the module are programmable by means of FPGA, which can be easy reconfigured from FLASH memory or directly via the VME interface.

1.1.1 Front Panel Inputs, Outputs

- 16 dedicated ECL inputs.
- 16 ECL configurable I/Os (two 8 bit groups).
- 16 dedicated ECL outputs.
- Two LEMO inputs (TTL and NIM level).
- Two LEMO outputs (TTL level).
- Two character alphanumeric display.
- Six LEDs.

1.1.2 VME Interface

- A32, D32 single cycle access (FPGA and CPLD).
- BT32, BT64 block transfer to and from memory (FPGA), optional.
- Two hexadecimal rotary switches for VME address offset (8 bit).
- FPGA I/O connection over VME P2 connector, optional.

1.1.3 Board Resources

- Front Panel I/O connectors.
- I/O Level converter.
- XILINX Vitex-4 FPGA.
- 256 K x 16 asynchronous RAM.
- VME bus transceivers.
- Two 16 channel connectors for Logic Analyzer.
- Power supply for voltages: 1.2V, 2.5V, 3.3V, 5V and -5.2V.
- Free programmable 2 character display.
- Six front panel LEDs.

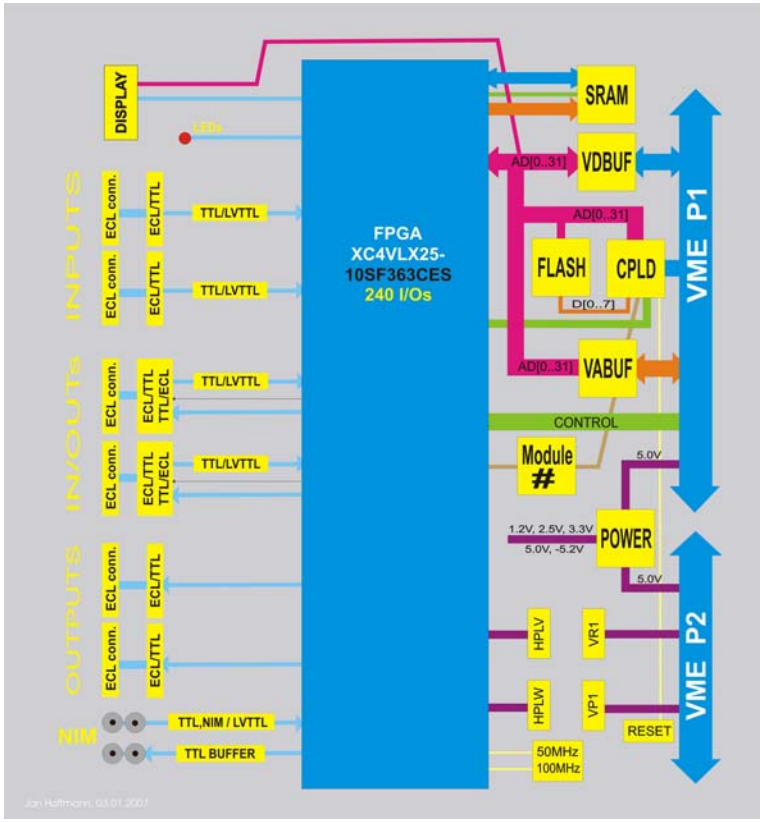
1.1.4 FPGA configuration

- Flash memory for configuration after power up.
- Direct configuration over VME.
- JTAG interface.

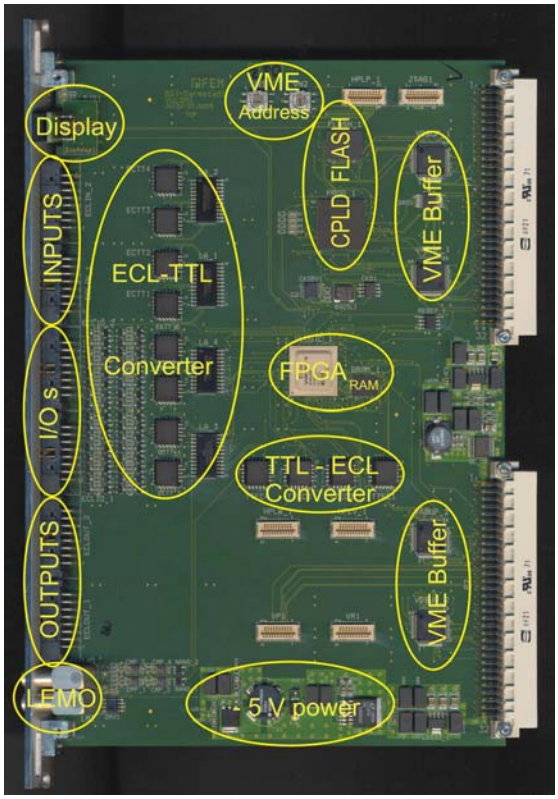
1.1.5 CPLD functions

- Simple VME interface.
    - Direct FPGA configuration.
    - FLASH reprogramming.
    - Reload command for FPGA.
- Configuration of CPLD over JTAG interface only.

1.2 Block diagram



Board Layout



1.3 Technical Data:

1.3.1 FPGA

- Type VIRTEX4LX25
- 24192 logic cells
- 21504 flip-flops
- 172032 RAM bits
- 8 digital clock managers (DCM)
- 7819520 configuration bits
- 363 balls BGA, 17x17 mm
- 240 I/Os

1.3.2 CPLD for FPGA configuration

- Type XCR3256
- 256 macro-cells
- 164 I/Os
- 256 balls BGA, 17x 17 mm

1.3.3 Memory (Asynchronous SRAM)

- Type K6R4016V
- 256K x 16 bit organization
- 10 ns access time
- 48 balls TBGA, 7x9 mm

1.3.4 FLASH Memory for FPGA configuration

- Type MT28F640
- 64 Megabit
- 64 ball BGA

1.3.5 VME Buffer/Register

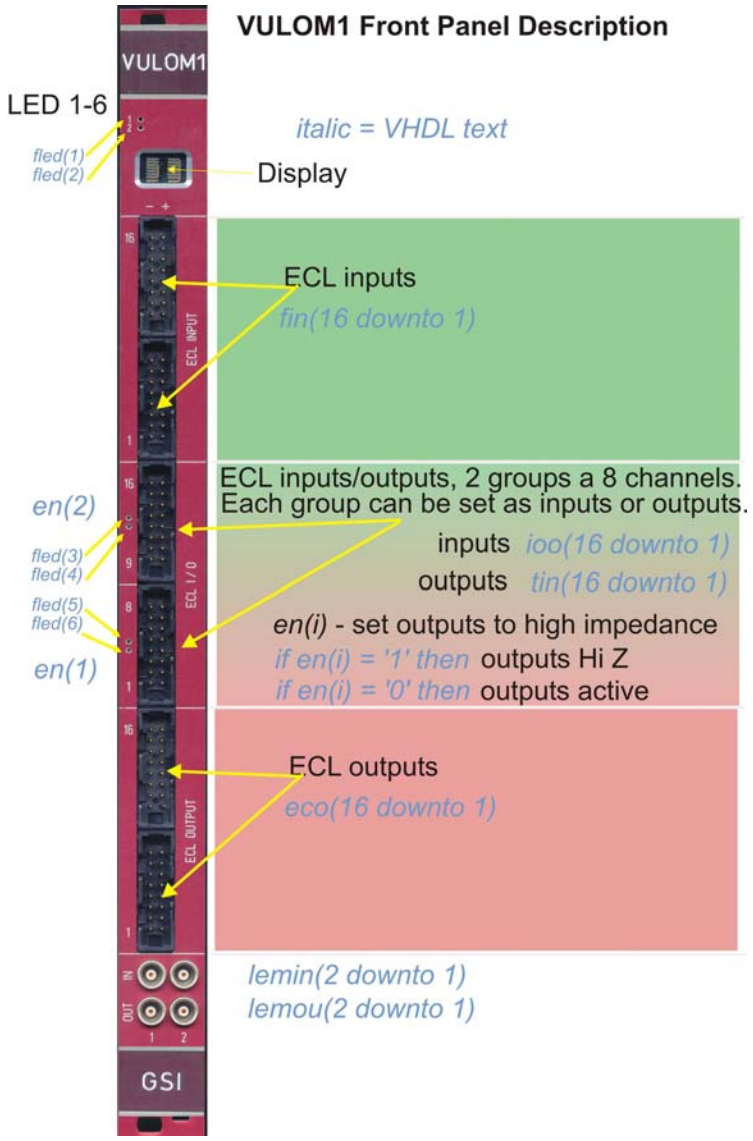
- Type SN74LVTH18502

1.3.6 Power Supply Requirements:

- VULOM 1 requires +5V supply only. All other voltages are generated on board:
    - o +3. V and –5.2V over DC-DC converter.
    - o +2.5V and + 1.2V over linear regulator.
- Current consumption is 2.9 A.

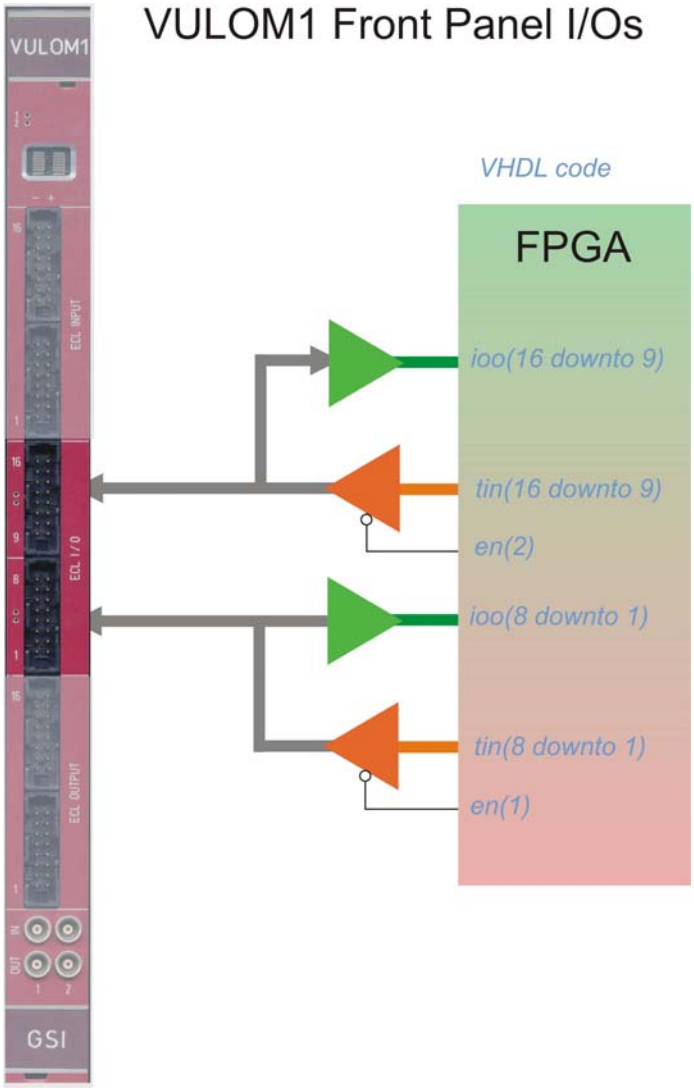
Warning: On power up before start of DC-DC converter the module needs ca. 7 A of current.

1.4 Front Panel.




```
entity vlogic_1 is
        Port (
--..... Front panel Controll Signals .....
        eco     :out std_logic_vector(16 downto 1);--  signals to ECL output (1 is the lower connector of ECL OUT)
        en      :out std_logic_vector(2 downto 1);--  ECL enable (EN1 for ch. 1-8, EN2 for ch. 9-16)
        fin     :in std_logic_vector(16 downto 1);--  signals from ECL input (1 is at the lower connector of ECL IN)
        ioo     :in std_logic_vector(16 downto 1);--  signals ioo from ECL I/O (1 is at the lower connector)
        tin     :inout std_logic_vector(16 downto 1);-- output signals to ECL I/O (1 is at the lower connector)
        lemin   :in std_logic_vector(2 downto 1);--  signals from LEMO  upper
        lemou   :out std_logic_vector(2 downto 1);--  signals to LEMO     lower
        fled    : out std_logic_vector(6 downto 1);--  Front panel LEDs
```

VHDL code example for front panel inputs and outputs.



Input – output function.

1.5 FPGA, CPLD configuration.

After power up the configuration program, if available, will be loaded from FLASH memory to FPGA with assistance of CPLD. The FPGA can also be reconfigured over VME program "restart". To load FLASH memory over VME use "progflash" program (for examples see section 1.8).

No	Resource	Address hex	Function
1	CSRR0	MK80 0000	Control and status register for reconfiguration (8 bit)
2	CSRR1	MK80 0004	Data register for direct reconfiguration over VME (8 bit)
3	FLASH	MKC0 0000-MKCF FFFC	FLASH memory (8 bit) 8 windows 8 MBit each *

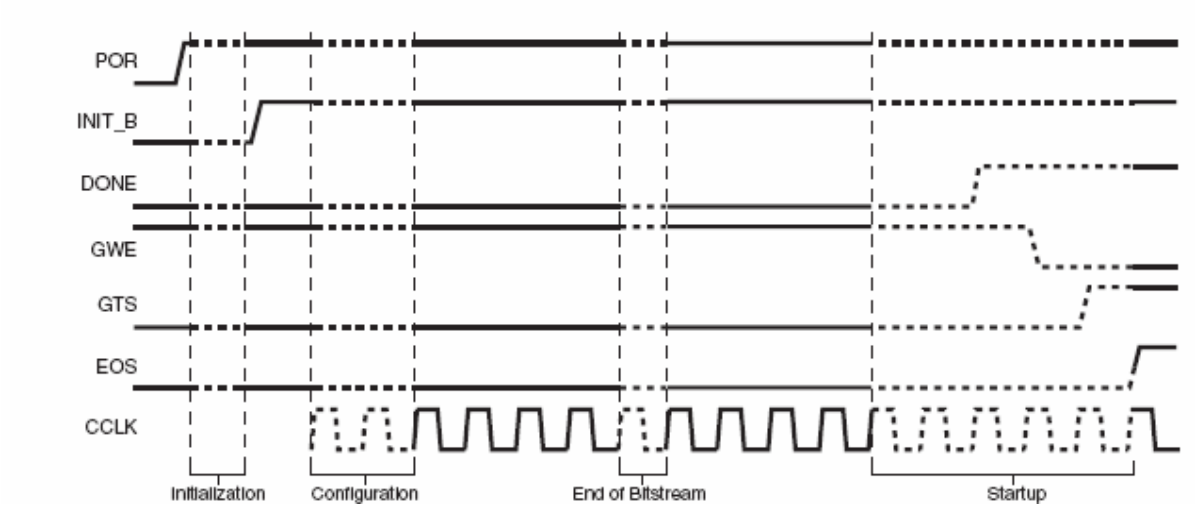
VME addresses of CPLD. M and K are VME module number, (M is set with VN2, K is set with VN1).

1.5.1 CSRR0 Control and Status register.

I/O	7	6	5	4	3	2	1	0
Wr	NOOP	NOOP	NOOP	VPROG	MRES	FL 21	FL 20	FL 19
Rd	NOOP	INIT	DONE	VPROG	MRES	FL 21	FL 20	FL 19

1. NOOP, no operation.
2. INIT, FPGA output. Low after reset (MRES) means that FPGA is not ready for reconfiguration (memory is not cleared). Low after reconfiguration means that there was an error.
3. DONE, FPGA output. Low means that reconfiguration is not finished correctly.
4. VPROG, if "1" together with MRES then direct reconfiguration over VME is started.
5. MRES, write "1" to start reconfiguration, together with VPROG="1" for direct VME reconfiguration, or when VPROG="0" then reconfiguration from FLASH memory.
6. FL20...FL19, FLASH memory address bit 21...19 for address offset selection, 8 x 8 MBit.

Warning: If reconfiguration doesn't successes then reconfigure once again or reconfigure from FLASH or switch power OFF.



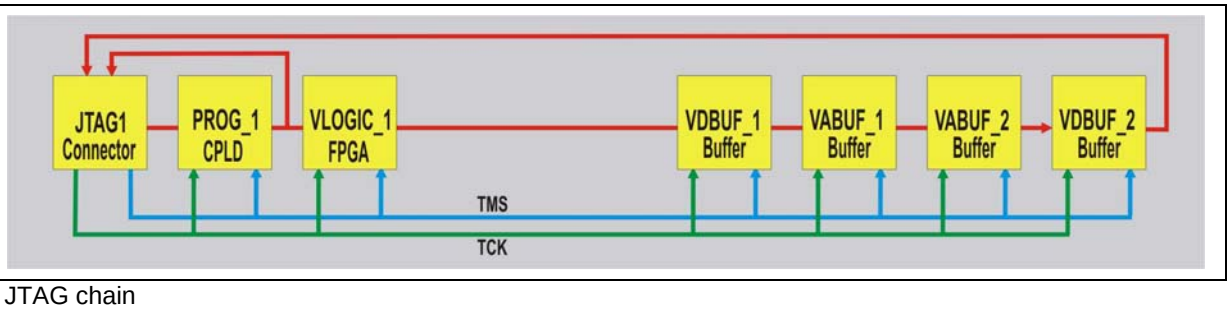
Configuration Signal Sequencing

A mismatch between the key in the encrypted bit stream and the key stored in the device causes configuration to fail with the INIT pin remaining High and the DONE pin remaining Low. The device does not become active and no damage to the device results. INIT_B is an open drain active Low output indicating whether a CRC error occurred during configuration: 0 = CRC error, 1 = No CRC error.
DONE, Active High signal indicating configuration is complete, `0` = FPGA not configured, `1` = FPGA configured

*For more details see **UG071, "VIRTEX 4 Configuration Guide."***

1.5.2 JTAG configuration.

Over JTAG interface both CPLD and FPGA can be configured.



JTAG chain

1.6 FPGA VME Resources.

The FPGA can be accessed over VME. The VME addresses are decoded in VMELOGIC sub design.

No	Resource	Address hex	Function
1	Space 1	MK0X XXXX	Four Megabyte address space
2	Space 2	MK4X XXXX	Four Megabyte address space

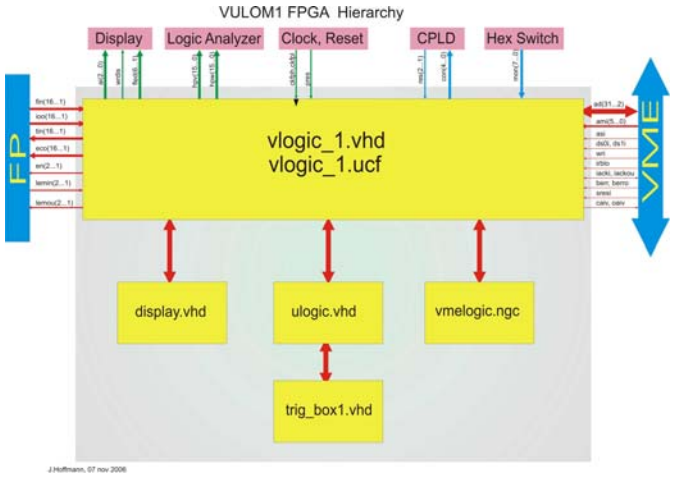
M and K are VME module number and corresponds to bit 31-24 of VME address. (M is set with VN2 switch and K is set with VN1 switch).
X are address bits for Space 1 and Space 2 (bit 21 ... bit 2).

1.7 Design

1.7.1 FPGA Signals

No	Signal Name	Description
3	AD[31…0]	VME address/data bus, internal
4	AMI[5..0]	VME address modifier
5	DS0I, DS1I, ASI, WRI, SRESI	VME control signals
6	CAIV, OAIV	VME address buffer/register control signals
7	IACKII, IACKOU, IRBLO	VME interrupt control signals
8	BERRO, BERR, BLTACK	VME bus error, (EUROGRAM experiment signal)
9	RES1, RES2, PRES	Reset signals
10	CKFPL, CKFPH	Clock 50 MHz, clock 100 MHz
11	MON[7…0]	Module number, connected to VN2, VN1 hexadecimal switch
12	CON[15…0]	Connection to CPLD
13	IOO[16…1]	Front panel differential ECL I/O (inputs)
14	TIN[16…1]	Front panel differential ECL I/O (outputs)
15	EN1, EN2	Enable signals for TIN outputs (1 set TIN to high Z)
16	ECO[16…1]	Front panel differential ECL outputs, lowest 16 channels
17	FIN[16…1]	Front panel differential ECL inputs, upper 16 channels
18	FLED[6…1], WRDIS, AI1, AI0	Front panel LEDs, write display, display address bits
19	LEMIN[2…1]], LEMOU[2…1]	LEMO input, output
20	SAD[17...0], SDA[15...0]	Asynchronous RAM, data, address bus
21	SWE, SOE, SCS	Asynchronous RAM control signals
22	HPV[15…0], HPW[15…0]	Logic analyzer connection

1.7.2 Design hierarchy example.



1.8 Program handling examples.

VN2 switch shall be 0 (address bit 31 to 28)

Erase flash, flash shall be erased before new program can be written.
>>> eraseflash 5 0 7

Program flash, writes a configuration file into FPGA.
>>> progflash 5 0 vlogic_1.rbt

Verify flash, reads FLACH contents and compares with file vlogic_1.rbt.
>>> veriflash 5 0 vlogic_1.rbt

Load FPGA configuration file vlogic_1.rbt directly over VME into FPGA and starts FPGA.
>>> loadfpga 5 vlogic_4.rbt

Reload FPGA with program from flash.
>>> restart 5 0

5 - VME module number (bit 24...27) set with hex. Switch VN1
0 7 - block number (block # 0...7) begin block, end block (FLASH has 8 blocks a 8MBytes)
vlogic_1.rbt - configuration file name.