MuBSy
Id.: VME-TRIG
Version: 1.2
Date: October 28, 1992
Revised: October 28, 1992

Trigger Module Description

H.G. Essel, J. Hoffmann, M. Richter, D. Schall

October 28, 1992

GSI, Gesellschaft für Schwerionenforschung mbH
Planckstraße 1, D-64291 Darmstadt
Germany
Tel. (0 6159) 71–0

Chapter 1

Trigger and Synchronization (TRIG)

1.1 Trigger and Synchronization

1.1.1 Trigger Tasks

Introduction

The Trigger Modules connected via the Trigger Bus have to guarantee together with the FEPs and the ROCs a correct inhibition of ADC gates and TDC starts during conversion and read-out time as well as the collection of corresponding subevents to the complete event by the EB. The Trigger Modules are either integrated into the EBI, AEB-VSB-Interface in FASTBUS, or into a CAMAC or VME single module.

There is just one dedicated Trigger Module in the whole system, called Master Trigger Module. Only this module accepts external triggers and performs Fast Clear (FC). It controlls also the GO line of the Trigger Bus (TBUS) thus starting or stopping the data taking in the whole system.

There are four Master Trigger ECL-inputs available on the front panel to select a specific trigger type. Using these four coded trigger inputs 15 different trigger types (1 - 15) can be distinguished.

Event Synchronization

The first of the four Master Triggers starts a trigger acceptance time window (GTIME) in the Master Trigger Module. To be accepted other triggers must arrive during this time. The GTIME is adjustable within 50 - 500 ns limits by means of on-board switch H2. The duration of the trigger inputs must be longer than 30 ns. The four inputs set four flip-flops to keep this trigger information until the Total Dead Time (TDT) on the Trigger Bus is cleared. The flip-flop outputs of the Master Trigger Module are sent via four Trigger Bus lines to all Trigger Modules in the

system from where they are readable through each Status Register. These four bits might be used by the ROCs to select an appropriate read-out procedure. The front panel ECL-signal Master Trigger (MT) with a duration of 50 - 500 ns (adjustable by on-board switch H1) is produced starting with the first Master Trigger input.

At the end of the GTIME that is calculated separetly in each Trigger Module the local Dead Time FF is set in each unit. The Total Dead Time (TDT) line of the Trigger Bus represents the wired OR of the local Dead Time FF of each Trigger Module. It is available as a front panel ECL-signal and as a bit in the Status Register of each Trigger Module.

With the first of the four Master Trigger signals a preprogrammable conversion time window (CTIME) (in 100 ns steps up to 6553.6 μs) is started in each trigger module individually. The length of the CTIME can be set by program individually in each Trigger Module.

At the end of its CTIME each Trigger Module sets the Start-of-Read-out (SOR) and interrupt signals to its ROC (only if no Fast Clear had stopped the CTIME). The interrupt is set in those Trigger Modules that have interrupt enable bit set in their Control Registers. In case of Fastbus an interrupt is sent via the EBI module to the AEB. In case of CAMAC this is done by asserting a LAM, in case of VME a VME interrupt is initiated. When working with CBV CAMAC module the LAM produces a VSB interrupt (if enabled) in the FEP. In addition, the interrupt bit is set in the Trigger Module's Status Register on which the ROC might poll. Now the ROC or the FEP in case of CBV module starts its read-out procedure.

The duration of the conversion time (CTIME) preprogrammmed in the trigger module must be longer by 100 ns than the gate time (GTIME) that was set by switch H2 in this unit. There is no hardware check on these settings! The restriction must be taken into account by the software initialization of the Trigger Modules.

Event Rejection

In case of necessary data flow reduction a fast and/or slow mechanisms of event rejection are foreseen.

The Fast Clear method can be initiated in Master Trigger only. Together with the GTIME the Master Trigger Module starts the fast clear acceptance window (FCATIME) preprogrammed in 100 ns steps up to 6553.6 μs. During this time an eventuall Reject pulse obtained by this unit produces a Fast Clear signal distributed over specific Trigger Bus line, to all Trigger modules. This signal resets the local Dead Time FF as well as a started CTIME in all Trigger Modules without interrupting a read-out processor, i.e. the trigger is ignored as if it had never appeared. A Fast Clear ECL pulse of 50 - 500 ns duration (adjustable by on-board switch H4) is available

on the front panel and can be fed into the Fast Clear inputs of the ADCs or TDCs. After a fixed settle down time (100 ns - 50 μs adjustable by on-board switch H3 in each module) the Total Dead Time line of the Trigger Bus is released and the system is now ready again to accept a new event trigger. These events never appear in the event data flow and are not counted by the event counters installed in each Trigger Module of the system.

The duration of fast clear acceptance time window (FCATIME) of the Master Trigger Module must be shorter than the shortest conversion time (CTIME) preprogrammed in the system. However, the FCATIME must be longer by 100 ns than the GTIME set in the module by switch H2. There is no hardware check on these settings! The restriction must be taken into account by the software initialization of the Trigger Modules.

The slow rejection of event can be initiated in any Trigger. During the CTIME or the read-out time each ROC or the FEP in case of a CBV module may detect invalid data and assert the Reject bit in its Trigger Module's Status Register. The Reject ECL-input from the front panel may also be used for this purpose. All Trigger Modules receive this Reject signal via the Subevent Invalid Trigger Bus line. Each ROC or the FEP in case of a CBV module can read this bit from its Trigger Module's Status Register. If the local CTIME is still in progress a Fast Clear signal is generated also as a front panel ECL pulse with 50 - 500 ns duration (adjustable by on-board switch H4) which can be fed into the Fast Clear inputs of the ADCs or TDCs. The SI signal stops the CTIME of all Trigger Modules where it is not yet timed out, to interrupt the ROC immediately.

Each Trigger Module can set or reset the Delay Interrupt line on the Trigger Bus by setting the corresponding bit in its Status Register. This bit is ORed on the Trigger Bus line 'Delay Interrupt'. The bit can be cleared by setting the Clear Delay Interrupt bit in the Status Register. The ECL Delay Interrupt Input level from the front panel of each Trigger Module is ORed to the Trigger Bus line 'Delay Interrupt'. The Delay Interrupt Trigger Bus line can be read from the Status Register. When the Delay Interrupt Trigger Bus line is set the Start of Read-out, and the Interrupt of the ROC or FEP, will be set if the local CTIME AND the Delay Interrupt disappeared. If the local CTIME disappeared already before the Delay Interrupt was set the interrupt is set 'normally' at the end of the CTIME and the later coming Delay Interrupt is ignored. The Delay Interrupt is cleared by setting the Subevent Invalid Trigger Bus line (Reject). With this mechanism one or more ROCs or FEPs can prevent others from the read-out of their modules by calculating Reject conditions during the Delay Interrupt time and setting the Reject Status Register bit in case of Reject.

At the end of the read-out time each ROC must sent a complete subevent with valid data or at least a subevent header with the Reject bit set. Each ROC may then set the Fast Clear bit in the Status Register for clearing of all ADCs or TDCs which are not read out before. This Fast Clear bit produces a pulse of 50 - 500 ns duration (adjustable by on-board switch H4) on the Fast Clear ECL-output at the front panel. This Fast Clear is not propagated through the Trigger Bus

but is used for local clear only. After data handling each ROC must reset the Dead Time FF locally in its Trigger Module by setting the Clear Dead Time bit in its Status Register. With the disappearance of the ORed Total Dead Time Trigger Bus signal a new trigger can be accepted by the system.

Event Counter

To guarantee the synchronization of all Trigger Modules in the system a readable 5 bit event counter located in each Trigger Module is installed. The Master Trigger Module increments its event counter at the end of the FCATIME if no fast clear appears during this time. The four least significant bits of the counter of the Master Trigger Module is propagated via the Trigger Bus to all Trigger Modules. All other Trigger Modules increment their event counter at the end of their conversion time window (CTIME), but only if no FC appears via the Trigger Bus from the Master Trigger Module. Then they check their own counter against the four bits of the Trigger Bus. In any case of inequality a Trigger Module sets the readable bits 'Mismatch' and thereby 'Reject' in its Status Register by hardware. To take into account the propagation delays of the four counter bits on the Trigger Bus the CTIME should be set at least to the length of the FCATIME of the Master Trigger Module plus the propagation delay between the Master Trigger Module and the specific Trigger Module. The propagation delay is about 7 ns/m Trigger Bus cable.

Reset and Halt

A Reset signal is produced in each Trigger Module either on power-up or by software bit in the Control Register. It is propagated over the Trigger Bus clearing Interrupt Enable,Master Trigger select, GO and Trigger Enable bits in Control Registers of all Trigger Modules in the system. A Halt command (Go bit cleared) sets the Total Dead Time line of the Trigger Bus thus inhibiting the system. The event counters of all Trigger Modules are cleared by Reset also. (TDT-FF).

1.1.2 Trigger Signals and Time Windows

- Master Trigger 1 to 4 (MT1, MT2, MT3, MT4):
  Four Trigger Bus signals initiated by the experiment's fast trigger logic and produced by the Master Trigger. The leading edge of the first one is equivalent to the leading edge of Start signals for TDCs. The first Trigger initiates the Master Trigger (MT) output signal on the front panel and starts the CTIME in each Trigger Module.

- Master Trigger (MT):
  Master Trigger output on the front panel in ECL-logic. The duration of this signal is 50 - 500 ns (adjustable by on-board switch H1). It is set with the first of the Master Trigger (MT1-MT4). This is the pulse with which all converters in the system begin digitizing the analog signals from the experiment, i.e. the ADC gate or TDC start.

- Conversion Time Window (CTIME):
  It starts with the first Master Trigger (MT1-MT4) signal and it is active as long as the the slowest converter served by Trigger Module needs time for conversion. It is programmable in 100 ns steps up to 6553.6 μs. Its length must be at least equal to the length of the FCATIME of the Master Trigger Module plus the propagation delay between the Master Trigger Module and the specific Trigger Module. The propagation delay is about 7 ns/m Trigger Bus cable. It can be shortened by a Fast Clear (FC) signal.

- Start of Read-out (SOR):
  This pulse is triggered by the trailing edge of CTIME telling the ROCs to start the read-out of data from the converters. It is not produced if a FC signal was generated by the Master Trigger Module. It sets the flag in the Status Register of a Trigger Module. If the interrupt is enabled it produces an AEB interrupt in case of Fastbus, a VME interrupt in case of VME or a LAM in case of CBV and CVC.

- Delay Interrupt (DI):
  Any Trigger Module may set its Status Register bit Delay Interrupt which is ORed on the Trigger Bus line 'Delay Interrupt'. The ECL Delay Interrupt Input level from the front panel of each Trigger Module can also be ORed to the Trigger Bus line 'Delay Interrupt'. This signal delays the Start of Read-out, i.e. the interrupt of each module not yet interrupted. With this signal a ROC or a FEP can postpone the interrupt of all other processors during the evaluation of a Reject condition, thereby saving the read-out time of the other processors. The line is reseted by explicit setting the Delay Interrupt Clear bit in the Status Register or by the Reset and the Subevent Invalid Trigger Bus signals. The ECL Delay Interrupt Input signal must be cleare externally.

- Read-out Time ROC (RTR):
  This is the time period the ROC needs to read its crate.

- Fast Clear output (FC output):
  This pulse is produced by each Trigger Module in case of Fast Clear, Reject state or if the

local Fast Clear bit in the Status Register was set. It is a pulse of 50 - 500 ns duration (adjustable by on-board switch H4).

- Fast Clear Bus (FC Bus):
  This Trigger Bus signal is sent by the Master Trigger Module to all Trigger Modules to 'forget' an event. It is generated by the Master Trigger Module only if a Reject input appears within the FCATIME.

- Fast Clear Acceptance Time (FCATIME):
  It starts with the first Master Trigger (MT1-4) input signal. It is programmable in the range in 100 ns steps up to 6553.6 μs. During this time a Reject input signal in the Master Trigger Module causes a fast clear signal on the Trigger Bus forcing all Trigger Modules to 'forget' the current event. Each Trigger Module produces therefore a local Fast Clear (FC) front panel pulse of 50 - 500 ns duration (adjustable by on-board switch H4).

- Reject (Rej):
  The Trigger Bus signal Subevent Invalid (SI) can be produced by any Trigger Module if the Reject bit in the Trigger Module's Status Register is set. This Status Register bit can be set by a front panel Reject ECL input signal (or together with the Mismatch bit in the Status Register or by software. It tells all other ROCs and FEPs that one ROC or FEP has detected an invalid subevent.

- Total Dead Time (TDT):
  It is the logical OR of MT1-4, CT and RTR. It is a Trigger Bus line (TDT) as well as a front panel ECL-Signal (TD) on each Trigger Module.

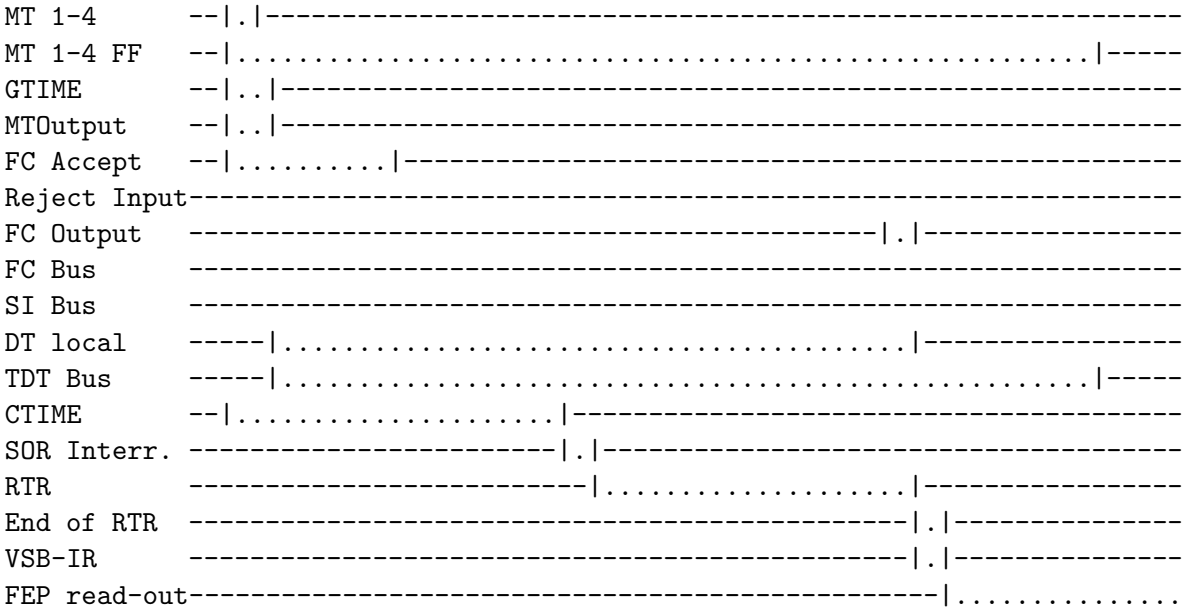
- RESET (RES):
  It resets all Trigger Modules on Trigger Bus, i.e. stops counters, clears the Status Register and sets the Halt state. It does not clear the preset counters (FCATIME and CTIME). This signal produces by either power up or by setting the corresponding bit in the Control Register of a Trigger Module.

- GO:
  This Trigger Bus line when disabled forces the whole system in the Halt state. The Halt state generates the TDT signal. The Halt state is set by either power up or software reset or by clearing the GO bit in the Control Register of a Trigger Module. The Go state is only set by setting the GO bit in a Master Trigger Module by program starting the data acquisition in the whole system.

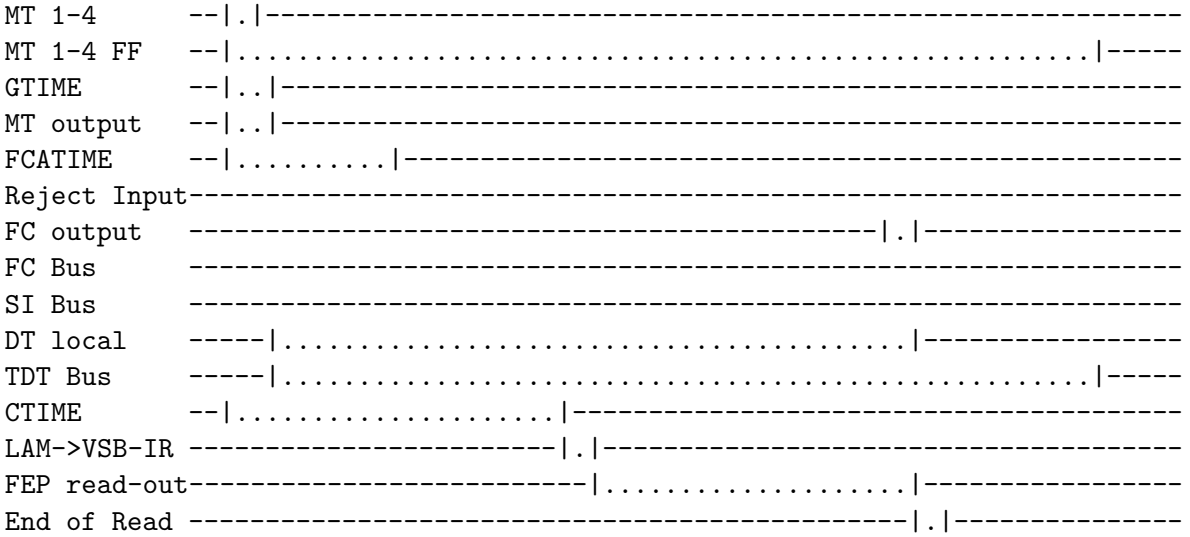
1.1.3 Trigger Sequence

The signals assumed to be active low are indicated by |....|

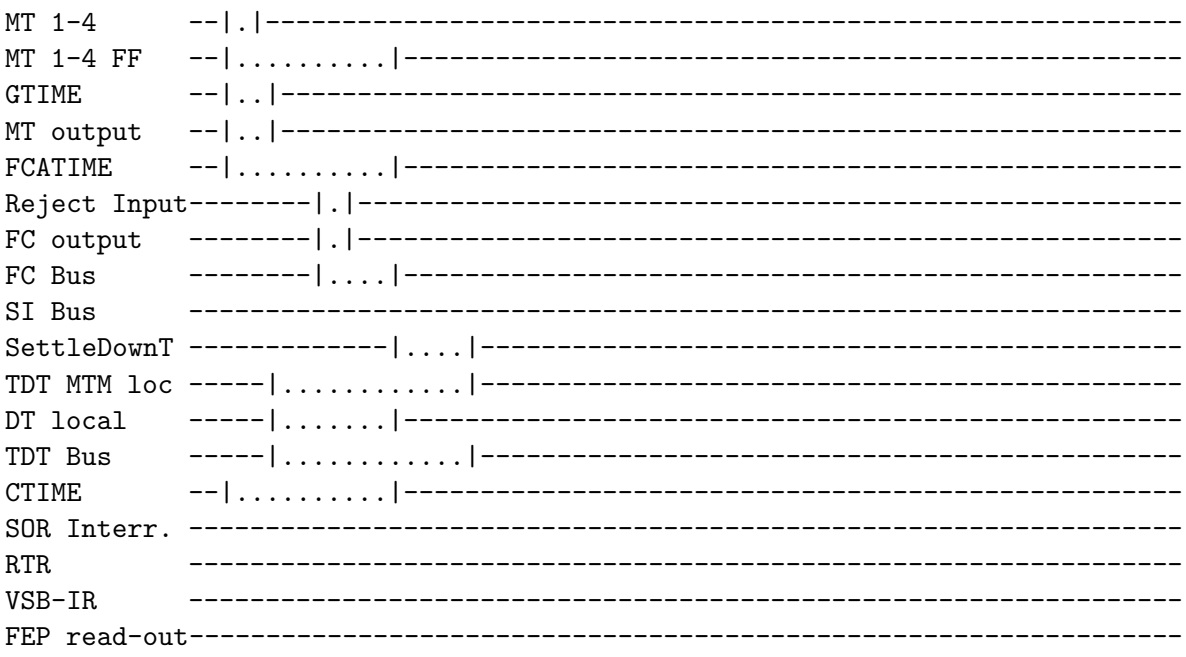
Normal trigger and read-out sequence (not CBV):



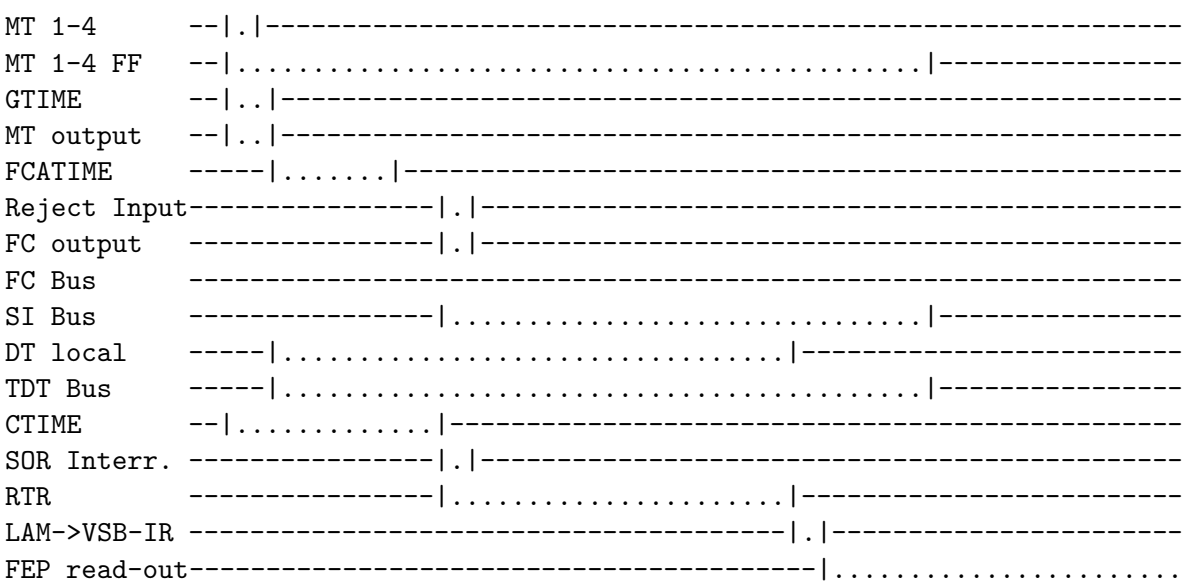
Normal trigger and read-out sequence for CBV :



Trigger and read-out sequence with Fast Clear:



Trigger and read-out sequence with subevent invalid SI:



1.1.4 Trigger Module Registers

Register Bit Layout

Status Register:

```
  16  15  14  13  12  11  10  9   8   7   6   5   4   3   2   1
-------------------------------------------------------------------
|EON|   |DI |EC5|EC4|EC3|EC2|EC1|SI |MIS|TDT|   |MT4|MT3|MT2|MT1|  Read
|               |               |               |               |
|               |               |               |               |
|E+I|DI |DI |IRQ|   |   |   |   |SI |   |DT | FC|MT4|MT3|MT2|MT1|  Write
|clr|set|clr|clr|   |   |   |   |   |   |clr|   |   |   |   |   |
-------------------------------------------------------------------
```

Status Register bits:

- MT1-MT4:
  'Master Trigger' 1 to 4 Trigger Bus lines. The coded Master Trigger set in the Master Trigger Module inputs from the experiment's electronic. Can be set by program in the Master Trigger Module at any time. Cleared by RESET or at the end of TDT.

- FC:
  Fast Clear pulse of 50 - 500 ns duration (adjustable by on-board switch H4) available on local ECL front panel output after writing a 1. This signal is not bussed to other Trigger Modules. It does not set or reset anything except the front panel pulse to clear ADCs or TDCs not read out before.

- TDT:
  Common 'Total Dead Time' Trigger Bus line status. Cleared by RESET or by DTclr in all Trigger Modules.

- DT Clr:
  Clear local 'Dead Time' by writing a 1.

- MIS:
  'Mismatch' status. Occurs on Event Counter mismatch. Cleared by RESET.

- SI:
  Subevent Invalid Line of the Trigger Bus. Activated by writing a 1. If done within FCA time performs fast clear.

- EC1-EC5:
  Local 'Event Counter' bits 1 to 5. Incremented at the end of CTIME if no Fast Clear

(FC) came from the Master Trigger Module. In the Master Module it is incremented at the end of the Fast Clear Acceptance Time (FCATIME) if no REJECT was set. Cleared by RESET.

- DI:
  The 'Delay Interrupt' Trigger Bus line. Set by writting DIset=1 cleared by DIclr=1 in all modules with DI on. (the ECL Delay Interrupt Input signal must be cleared externally).

- EON:
  The data are ready for read out in this module. Cleared by RESET or by E+Iclr.

- E+I clr:
  Clear event and 'Interrupt' in the Trigger Module by writing a 1. In case of VME module also clears IRQ* on the VME bus.

- IRQ clr:
  Used in VME standard only. Clears interrupt generator, used in case of error condition.

Control Register:

```
  16  15  14  13  12  11  10  9   8   7   6   5   4   3   2   1
-------------------------------------------------------------------
|   |   |   |   |   |   |   |   |   |   |   |   |   |MTM|GO |INT|  Read
|               |               |               |           ena|
|               |               |               |              |
|   |   |   |BUS|BUS|   |   |   |   |RES|MTM|HLT|INT|MTM|GO |INT|  Write
|   |   |   |dis|ena|   |   |   |   |   |dis|   |dis|ena|   |ena|
-------------------------------------------------------------------
```

Control Register bits:

- INT:
  Interrupt enabled in this Trigger Module when INT=1. Enebled by writting INTena=1, disabled by INTdis=1.
- RES:
  Reset the Trigger Module by writing a 1. Produces a Reset pulse in the Trigger Module and on the Trigger Bus Line thereby reseting all Trigger Modules. Produced by power up also.
- GO:
  GO Trigger Bus line status. In 'Go" state by writing GO=1, in 'Halt' state by writing HLT=1.
- MTM:
  Master Trigger Module. Selected by writing MTMena=1, disabled by writing MTMdis=1.

FCATIME Register:

Fast Clear Acceptance Time is programmable in 100 ns steps up to 6553.6 μs (= 16 bits) (read/write).

CTIME Register:

CTIME is programmable in 100 ns steps up to 6553.6 μs (= 16 bits)(read/write).

Registers Addresses

All FASTBUS trigger registers can be accessed from the AEB via internal EBI port bus and by the FEP. EBI addresses from AEB (baseaddr. = 0) are:

- status 3001000
- control 3001004
- FCA 3001008
- CVT 300100C

EBI addresses from E6 (Crate nr.1) are:

- status F2201000
- control F2201004
- FCA F2201008
- CVT F220100C

CAMAC trigger registers are red by F(0) and written by F(16) functions. Subaddresses A values are:

- status A(0)
- control A(1)
- FCA A(2)
- CVT A(3)

VME module registers can be accesed in extended addressing mode as follows:

- status 02000000
- control 02000004
- FCA 02000008
- CVT 0200000C

VME Interrupt Settings

Setting of the VME interrupt level IRQ*, interrupt ackowledge level INTACK* and of the interrupt vector value can be done by means of jumpers and the switch as shown in the chapter " Internal jumpers and switches".

1.1.5 Front Panel

Front Panel LEDs

```
-------------------------------------------------------------------------
|-5| Power                              |T1|                              |
|+5| Power                              |T2|Master Trigger Bus lines      |
|TE| TBUS terminator in                 |T3|        1 - 4                 |
|MT| Master Trigger Module, control bit |T4|                              |
|GO| Go, TBUS bit                       |  |                              |
|TD| Total Dead Time, TBUS bit          |MI|Mismatch, status bit          |
|IR| Interrupt request, status bit      |FC|Fast clear, TBUS line         |
|ID| Interrupt delay, TBUS line         |SI|Subevent invalid, status bit  |
-------------------------------------------------------------------------
```

Trigger Bus Connector

The Trigger Bus TBUS is a differentially driven bus (it is not an ECL bus!!). On the front panel it is represented by the 34-fold (17 pairs) flat cable connector with 3 pairs reserved for future use.

```
---------------------------------------
| Pin |     Describtion                |
---------------------------------------
| 1-2 | ID       Interrupt delay       |
| 3-4 | SI       Subevent invalid      |
| 5-6 | GO       Go                    |
| 7-8 | TDT      Total dead time       |
| 9-10| RESET    Reset                 |
|11-12| FC       Fast clear            |
|13-14| MT1                            |
|15-16| MT2      Master trigger lines  |
|17-18| MT3              1 - 4         |
|19-20| MT4                            |
|21-22| EC1                            |
|23-24| EC2      Event counter lines   |
|25-26| EC3              1 - 4         |
|27-28| EC4                            |
|29-30|                                |
|31-32|             Spare pairs        |
|33-34|                                |
---------------------------------------
```

ECL Front Panel I/O

The inputs/outputs available at the front panel of each Trigger Module are ECL differential standard signals. One 16 pin (8 pairs) flat cable connector for input and one for output are installed.

The ECL inputs are available on the upper 16 pin connector on the front panel of each trigger module.

Pin	Description	
1-2	T1	
3-4	T2	Trigger inputs
5-6	T3	1 - 4
7-8	T4	
9-10	REJECT	Reject
11-12		
13-14		
15-16	DI	Delay interrupt

The ECL outputs are available on the lower 16 pin connector on the front panel of each trigger module.

Pin	Description	
1-2	MT	Master trigger
3-4	FC	Fast clear
5-6	SOR	Start of readout
7-8	TDT	Total dead time
9-10	GO	Go bit
11-12	GO*	Go inverted
13-14		
15-16		

1.1.6 Internal Jumpers and Switches

There are 4 switches, 4 sliders each, that are installed on the trigger board in order shown below and enabling to set 4 important pulses. The sum of the constant value and of that switched on defines the duration of the pulse.

ECL MASTER TRIGGER PULSE SWITCH:

Switch H1

Installed on board	Added when slider on				TOTAL RANGE
	1	2	3	4	
ns	ns				ns
50	50	50	100	250	50 - 500

GATE TIME SWITCH:

Switch H2

Installed on board	Added by switch				TOTAL RANGE
	1	2	3	4	
ns	ns				ns
50	50	50	100	250	50 - 500

SETTLE DOWN TIME SWITCH:

Switch H3

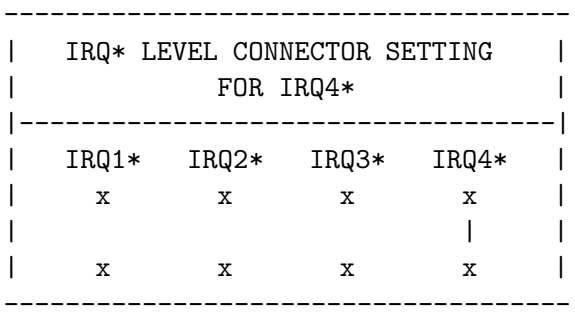
Installed on board	Added by switch				TOTAL RANGE
	1	2	3	4	
us	us				us
0.1	1.9	3	10	35	0.1 - 50

ECL CLEAR PULSE SWITCH:

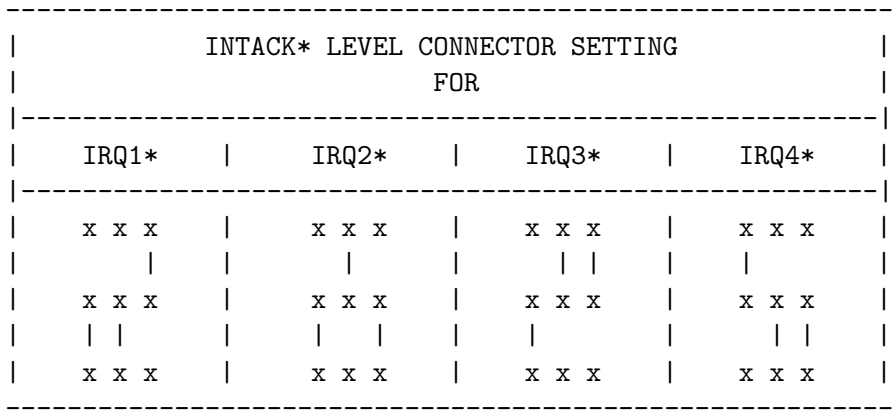
Switch H4

Installed on board	Added by switch				TOTAL RANGE
	1	2	3	4	
ns	ns				ns
50	50	50	100	250	50 - 500

VME IRQ* LEVEL JUMPER: The interrupt request level IRQ* in the VME module can be set by shortening the proper pins in the IRQ* LEVEL CONNECTORS row:



VME INTACK* LEVEL JUMPERS: The IRQ* level must correspond with setting for encoded address bits that are sent over the bus during the interrupt acnowledge cycle. This can be done by jumpers installed in the INTACK* LEVEL row:



VME INTERRUPT VECTOR SWITCH: The interrupt vector that is sent over the VME bus during the interrupt acknowledge cycle can be choosen by means of the INTERRUPT VECTOR SWITCH. Every single slider in "on" position activates the corresponding bit in the interrupt vector.

1.1.7 Cirquit Description

The FASTBUS trigger module is installed on the PCB located at the rear of the crate. The same PCB is used in the CAMAC module being connected to the dataway over an interface.
The VME module was designed as a new board, however, its trigger part is a copy of those in CAMAC and FASTBUS. Again, the trigger part communicates with the VME bus over an interface.
The performance of the trigger cirquit is controlled by:

- status register described in the manual on page 11 and shown in the diagram on page 10
- control register described in the manual on page 13 and shown in the diagram on page 11.
- fast clear acceptance time (FCATIME) register an internal register installed in two 74LS593 IC's shown on page 2 of the diagram.
- conversion time (CTIME) register an internal register installed in two 74LS593 IC's shown on page 3 of the diagram.

The commands used to acces the registers are decoded in the commands decoder FDEC shown on page 11 of the diagram and the necessary addresses or NAFs are described on page 14 of this manual. For better understanding of the trigger work it should be noted that the module represents a part of the trigger system organized around the trigger bus. Because of that all trigger bus signals used in the module are the output signals from the bus. This rule is valid in the single trigger system also.

Normal trigger sequence acc to diagram 1 and 2

The sequence starts with registration of the rising edge of any trigger pulse that is supplied either by software /10-8G/ or by ECL input /8-4G/. The triggers that are registered in the trigger register of the master unit /1-4A:E/ are ORed /1-3F/and start the GTIME* /1-9D/ together with the master trigger output MT /1-9G/.
The GTIME* pulse starts the measurement of the FCATIME*/2-2B/ and CTIME* /3-1B/. In both cases the measurement is performed by counting the clock pulses /4-4B/ in 16 bit counters built of two 74LS593 ICs /2-5E:H for FCA and 3-5E:H for CTIME*/. The rising edge of the CTIME* pulse sets the dead time flip-flop in the module /5-9E/. The signal DTIN produced by this flip-flop is sent on the trigger bus /7-6F/ to be ORed with the dead times of other triggers.If the interrupt was enabled in this module /11-6D/ the interrupt pulse /6-9B/ is set in parallel to the DTIN and to the start of read out ff /6-9C/. The INT and SOR signals can be delayed by setting the delay interrupt bit DIIN in the status register /10-9C/ of any trigger on the bus. The DIIN is first sent on the trigger bus /7-6H/ and used later as the DIOUT signal /6-0B/ in all trigger modules. At the end of the read-out routine the read out processor prepares the trigger module for the next event by writting E+I clr and DT clr in the status register /10-8E

and 10-9F/. E+I clr pulse resets the event ff /6-2C/ and interrupt ff /6-4C/while the dead time clr pulse clears the dead time ff /5-5D/. Together with the last dead time in the slowest module of the system the total dead time line on the trigger bus is cleared. This clears the trigger register in the master trigger module /1-4A:E/. The events are counted in the event counter shown on page 9 of the diagram. The master counts at the falling edge of the FCATIME /9-0E/ while slaves at the end of the CTIME /9-0D/. The counters are compared in slave modules at the end of start of read-out pulse /9-1C/ to set the mismatch bit /9-9C/ in case of unequal contents of counters. The resulting MI bit lights the coresponding LED /4-6E/ and sets the bit in the status /10-0C/.

Fast clear sequence acc to diagram 3

The REJECT pulses that start the fast clear sequence come within the FCATIME either from the ECL input /8-5E/ or are sent per software /10-8F/. The time condition is arbitrated in the event reject section shown on page 6 of the diagram. If it is fullfilled the FCIN* pulse /6-8F/ is sent on the trigger bus. The related FCOUT* pulse received in each trigger module in the system stops the normal triggering sequence that was described above. This is done by clearing the FCATIME* /2-8B/, CTIME* /3-8B/ and DTIN* /5-9E/. The FCOUT produces the SC pulse that triggers the settle down time ff /5-5E/ thus expanding the local dead time DTIN /5-9E/ and disables the counting of the reseted event /9-0E/.

SI sequence acc to diagram 4

The REJECT pulse that comes after the FCATIME was ended results in the subevent invalid SI sequence. The SIOUT pulse that is produced at the beginning of the sequence cuts the CTIME measurement, if on /3-1A/ and triggers the settle down time ff /5-5E/. In parallel the SI LED is lighted /4-6D/ and SI bit in the status register is set /10-1C/.

Software trigger

To enable for proper asynchroneus software triggering the EP610 PLD chip was installed in the status register /10-4H:G/. The chip is loaded with the triggering combination of 4 least significant bits during the load status operation LSTAT*. It keeps this information as long as the current event is in progress. The software trigger sequence starts with presetting of the trigger register /1-4A:E/ immediatelly after the TDT was cleared. The hardware trigger is inhibited at that time. The timing that follows is the same as in the case of hardware trigger.

1.1.8 Testing

1. Inspect the board for:

```
- mechanical errors,
- mounting errors,
- settings of switches and jumpers,
- installation of terminators.
```

2. Apply the power.
3. Read and write the registers and counters checking for consistency.
4. Check LEDs for consistency with status and control registers.
5. Use logic analyzer to obtain the diagrams 1, 2, 3 of this manual.

```
- use test set-up and program from P. Liebold in case of
  CAMAC module
- use test set-up and program from D. Schall in case of VME,
- the FASTBUS modules can be tested as CAMAC units first
  and reconfigured for FASTBUS later.
```

6. integrate the module in multitriger system and check proper operation of event counters /mismatch - MI LED/ and fast or software clear /FC and SI/.

1.1.9 Troubleshooting

1. Check conditions in the crate /power supply, overload, overheating etc/.
2. Check installation of cables, terminators,switches and jumpers:

```
- the arrows on plugs and sockets must match,
- the first and last module on the trigger bus
  must be terminated /observe LEDs/,
- GTIME setting must be shorter than CTIME and FCATIME,
- in case of VME module the interrupt level jumper and
  the interrupt  acknowledge level jumper must match.
```

3. Check if only one master in the system.
4. Check GO, TDT, DI, FC, SI LEDs for proper operation.
5. Check if proper software in use:

```
- the sequence of hardware initialization,
          1. after power-up the system must be reseted,
          2. enable trigger bus in every unit,
          3. load regisers of all slaves,
          4. load registers of the master,
          5. write GO in the master unit.
- the values of GTIME, CV and FCA times:
          1. GTIME must be shorter than CV and FCA
          2. FCATIME in master module must be shorter than
             the shortest CVTIME in the system,
- the proper event read-out routine,
- the proper use of reset function,
- the proper use of TRIGBUSEN*.
```

6. contact EL/EX group representative.

Contents