CAMAC ECLine Model 4448 48-Bit Coincidence Register

* High density: 48 bits in a single-width CAMAC module.
* Low cost: with three times conventional density, per-bit cost decreases drastically.
* ECL inputs: 100 Ohm complementary inputs simplify total system.
* MWPC application: ideal in high-rate applications using cable delays.
* Analog sum output: three analog outputs (groups of 16 bits) permit fast majority decisions.
* Fast common gate: provides coincidence resolving time under 3 nsec.
* Fast clear: rejected events can be cleared in less than 5 nsec.

The LeCroy Model 4448 Coincidence Register ("pattern unit") offers fast storage capability at an unprecedented high density and low cost. Its complementary ECL line receiver input stage, compatible with inexpensive twisted-pair flat cable, makes it perfectly suitable for both small and large multiwire proportional chamber and hodoscope systems. The three fast analog outputs providing majority information are extremely useful in fast trigger decision applications.

The logic channels, which seek a coincidence between each input and a common fast gate input, provide coincidence resolving times under 3 nsec. Logical "l" data levels, representing the time coincidence between the common gate and the 48 inputs, are stored in a 48-bit fast buffer register for later readout under CAMAC commands. The facility of performing majority logic is provided by three front-panel summing outputs which are each driven by 16 logic channels. The output current of the summing circuit is proportional, in increments of 100 mV into 50 Ohm per register bit, to the number of coincidences stored in the register. Other operating features include a front-panel clear input, which responds to negative logic levels, and a built-in test mode.

High Density/Low Cost

The modern design and a new concept of input interconnection have resulted in a dramatic density increase over present designs. With 48 bits per slot, up to 1104 bits of fast coincidence registers can be housed in one CAMAC crate.

Besides the advantage of reducing the physical size of an experimental setup, high density cuts down CAMAC overhead and per-bit cost. This new system concept also permits substantial savings on interconnection costs.

MWPC Applications

Its high density and low cost per bit make the Model 4448 Coincidence Register well suited for multiwire proportional chamber work. Its complementary line receiver input stage is fully compatible with the LeCroy Model 7790 16-channel chamber card, as well as with most in-house designed MWPC amplifier-discriminators.

The simplicity of system setup obtained using the Models 7790 and 4448 is very attractive for small systems. It is also feasible for large systems in high-rate conditions where cable delays must be used to minimize deadtime.

High-speed readout of large systems can be performed through a dedicated controller using the LAM structure to skip empty modules. Encoded data is then transferred to the LeCroy Model 4299 memory module.

Hodoscope Applications

L In hodoscope applications, the Model 4448 Coincidence Register is used in conjunction with the Model 4416, a 16-channel 200 MHz updating discriminator with complementary ECL outputs.

In cases where cost is a primary consideration, the Model 4448 can be directly connected with the LeCroy Model 4415, a 16-channel, 80 MHz non-updating discriminator.

SPECIFICATIONS CAMAC Model 4448

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48-BIT COINCIDENCE REGISTER/PATTERN UNIT



 INPUT CHARACTERISTICS

 Number of Inputs:  48; all identical.
   100 Ohm direct-coupled; high impedance by simple user option.
   Reflections <10% for complementary ECL signal of 2 nsec risetime.
   Minimum width <4 nsec.
 Input Sensitivity:  +/-200 mV differential.

 Double-Pulse Resolution:  8 nsec max.; 6 nsec typical.

 Gate Input:  One; Lemo-type connector; 50 Ohm impedance; -600 mV or greater; min
   mum duration at full logic level (-750 mV), 3.0 nsec.

 Clear Input:  One; Lemo-type connector; -600 mV or greater,
   50 Ohm impedance; minimum duration 5 nsec;
   2 nsec settling time after clear.
 OUTPUT CHARACTERISTICS

 Summing Outputs:  3 identical: one for each of the three groups A, B, C of 16 bi
   -100 mV +/-5% into 50 Ohm is presented for each register latched in the
   corresponding group of 16.
   Maximum output into 50 Ohm, -0.7 volt corresponds to 7 set registers;
   risetime 3 nsec, delay of leading edge of summing output from leading
   edge of coincident input; 9 nsec.
 CAMAC COMMANDS

   Z or C: Clears registers during S2. (Used for special test feature option.)
   l: Inhibit gate input.
   FO-AO: Reads register A.
   FO-Al: Reads register B.
   FO-A2: Reads register C.
   F2-AO: Reads and clears register A.
   F2-Al: Reads and clears register B.
   F2-A2: Reads and clears register C.
   F9-AO: Clears register A.
   F9-Al: Clears register B.
   F9 A2: Clears register C.
   F8-(A0 + A1 + A2): fests LAM.
   F11A-(A0 + A1 + A2): Clears all registers.
   L: LAM: logic OR of all registers (switchable on or off for each
    register A, B or C).
 GENERAL
 Gate-Input Delay:  2.5 nsec typical.
 Coincidence Width:  2.5 nsec up, determined by input and gate pulse durations.
 Packaging:   CAMAC single-width module.
 Power Requirements:  +6 V: 400 mA
   -6 V: 1.9A
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