CAMAC Model 4434 32 Channel 24-Bit Latching Scaler

* High Density: 32 Scalers, 24 bit each, in a single width CAMAC Module
* Auxiliary Bus Output: for interconnection with external raster scan display
* Medium Counting Rate: 20 MHz
* Input Levels: complementary ECL or single ended TTL
* Common Load, Common Clear, Common Veto: on the Front Panel or via CAMAC Command
* LAM Generation
* Sequential or addressed readout

The LeCroy Model 4434 contains 32 channels of 24-bit scalers. Through the extensive use of LeCroy custom built hybrid circuits, the Model 4434 achieves a dramatic increase in channel density with a very low overall cost per channel.

Each channel is identical and is followed by an internal buffer which may be used to store and readout accumulated data independent of data acquisition.

Inputs to the 4434 are complementary ECL levels compatible with all ECLine modules. Single ended TTL levels are available as a factory option. Each scaler counts signals which have a dura- tion > 10 nsec and a maximum frequency of 20 MHz, assuming the module is not disabled by either the front panel veto or CAMAC Inhibit. However, a local double pulse resolution of 30 nsec is permitted. Receipt of a CAMAC or front panel Load command temporarily halts the scalers and transfers the contents to the internal buffer memory. The scalers may then be optionally cleared before counting is resumed.

Memory readout may take place at any time, independent of data acquisition, under standard CAMAC or Auxiliary Data Bus control. In either case, readout can be performed both sequentially or randomly.

The Auxiliary Bus organization is designed to permit connection of up to 16 modules to the same bus.

CAMAC Model 4434 32 Channel 24-Bit Latching Scaler
Specifications

INPUT CHARACTERISTICS	
Signal Inputs:	32, in two 2 x 17-pin front panel connectors, BERG 7578D-101-34.
Input Levels:	Differential ECL (Factory option is available to accept TTL single-ended inputs with the scaler incrementing on the negative going transition).
Input Impedance:	110 Ohm pin-to-pin with differential ECL, 560 Ohm to + 5 V for TTL single-ended inputs.
Input Pulse Width:	10 nsec minimum.
Double Pulse Resolution:	Less than 30 nsec.
Maximum Frequency:	> 20 MHz.
Maximum Instantaneous Rate:	>30 MHz.
COMMAND INPUTS	

General:	The LOAD, CLEAR and VETO inputs each have a single front panel Lemo-type connector; a common side-switch selects either negative going NIM or TTL levels, input impedance 50 Ohm for NIM pulses-, 50 Ohm AC and 100 Ohm DC to + 5 V for TTL pulses.
Load Input:	A LOAD pulse with > 1 0 nsec width will disable inputs for 220 nsec and shift the scaler contents into a 32-word x 24-bit buffer; the LOAD command can optionally generate a LAM on the CAMAC dataway and also prepare the memory for readout by loading the starting subaddress (FA) and readout number (RN) previously defined by a CAMAC F(16) or Z; a front panel LED (RDE, Readout Enabled) is lit in recognition of a Load command.
Clear Input:	A CLEAR pulse with >20 nsec width will disable inputs for a duration of approximately 100 nsec and clear the 32 scalers.
Veto Input:	Disables inputs for the duration of the VETO (action identical to CAMAC INHIBIT).
CAMAC COMMANDS AND FUNCTIONS	
Note: The following notation is used in this section: CR: Command Register; loaded by F(16) FA: First Address to be read RN: Readout Number; defines how many channels (minus one) have to be read in the module.	
Z:	Initialize the unit at S2, i.e. all scalers, buffer and LAM are cleared as well as register CR.
C:	Clear all scalers at S2. All scaler inputs are inhibited during CAMAC INHIBIT command" the action is identical to that of the front panel VETO input.
X:	A X= 1 response is generated in recognition of any valid function.
Q:	A Q= 1 response is generated in recognition of any executable function.
L:	A Look-At-Me signal can be generated according to several possible options described in the "Option Switches" section below.
N-F(O)-A(O):	Generates readout of the selected channel; F(O) can be executed and a Q = 1 response will be provided under the following conditions: a) Side switch LAD (Latching Disable) = ON: always if the LED RDE (Readout Enabled) is ON. b) Side switch LAD = OFF: only after a LOAD has been performed and as long as the readout of the given number of channels had not been completed.
N-F(2)-A(O):	Sequential data readout with auto-increment of the address; F(2) can be exe- cuted and a Q= 1 response will be provided independent of the Latching Disable switch position, if a LOAD has been previously performed, and as long as the readout of the given number of channels has not yet been completed. Note: if the number of scalers to be read is RN + 1 > 32-FA then the readout, after address 31, will continue with addresses 0, 1, 2, etc. until RN + 1 chan- nels have been read.
N-F(8)-(O):	Test LAM: Q = 1 response is generated when LAM is ON.
N-F(10)-A(O):	Test and clear LAM; a Q = 1 response is generated when LAM is ON. LAM is cleared at S2. Note: LAM goes on again after F(10) in the following cases: a) Switch LOF (LAM at Overflow) = ON and scaler not cleared. b) Switch LDR (LAM Data Ready)= ON and data readout not finished.
N-F(l6)-A(O):	Load register CR (Command Register); F(16) can always be executed and a Q= 1 response is generated.
FA:	First Address to be read.

RN:	Readout Number-, defines how many channels (minus one) have to be read starting from the address FA; after a Z command, RN is set to 31 and FA to 0.
T	Test-, when T = 1 permanently inhibits signal inputs-, increments at S2 all scalers by one count; after a Z command T = 0.
LD:	Load; LD = 1 performs a load if switch LAD (Latching Disable) = OFF; after 0.8 usec the module will be ready for readout; enables functions F(O) and F(2).
CL:	Clear; CL = 1 clears all the 32 scalers.
RD:	Readout enable; RD = 1 prepares the module for readout, does not require a LOAD; readout can be started after 0.8 usec.
BD:	Bus Disable; BD= 1 disables the Auxiliary Bus readout; after a Z command BD = 0.
OPTION SWITCHES	
A set of side accessible switches allows the user to select different options as follows:	
LAD:	Latching Disable; when ON the module works as a normal non-latching scaler.
OVF:	Overflow decides whether an overflow condition occurs when bit 16 of any scaler is ON or when bit 24 is ON.
LCO:	LCO:
LOF:	LAM at Overflow; a LAM is generated when at least one channel reaches the overflow set value.
LRE:	LAM at Readout Enable; a LAM is generated after a readout request.
LDR:	LAM Data Ready-, a LAM is generated after a readout request and as long as there are data to be read.
BAD:	4-bit Bus Address-, defines module address in the auxiliary bus.
VBR:	Veto by Bus Readout; enables a veto of all scaler inputs during the loading of the auxiliary bus output registers (< 200 nsec).
NIM/TTL:	Decides pulse standard accepted by inputs LOAD, CLEAR and VETO: NIM: 0=0 mA 1 = - 12MA TTL: 0= +2.5 V 1 = + 0.5 V
AUXILIARY BUS	
A total of 16 LeCroy Model 4434 Modules may be interfaced to an auxiliary bus via a front panel 34-pin connector. The auxiliary bus must end in an indepen- dent dedicated controller. Use of the auxiliary bus permits addressed readout of the scaler contents independent of CAMAC operations for applications such as raster scan display.	
GENERAL	
Packaging:	Single width CAMAC standard module.
Power Consumption:	TTL-Version ECL-Version +6V 2.8 A 3.1 A -6V 40 mA 400 mA

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