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4418/T 8-INPUT SPECTROSCOPY GRADE TDC
8 Input Channels in a Single-Width CAMAC Module Spectroscopy Grade Performance with Excellent Integral and Differential Linearity
High Speed ECL Readout Logic
Fast Conversion: 3 µsec for Every Valid Input Channel
FOR HIGH RESOLUTION CHARGE, VOLTAGE AND TIME MEASUREMENTS
The Silena International Model 4418T Time-to-Digital Converter each has 8 channels of high resolution This modules is compatible with LeCroy FERA and ECLbus systems.
The module is highly stable, offering superior integral and differential linearity performance, as well as fast conversion and readout capabilities.
The Model 4418T has been designed for use in a variety of experimental situations that employ many TDC channels to perform high resolution, high stability data acquisition.

FUNCTIONAL DESCRIPTION

The Model 4418T is an 8-channel Common Start Time-to-Digital converter. It has a full scale of 200 nsec with a least count of 50 psec. This module includes an upper level and lower level discriminator for time window mea surements. Digitized data are available first on the front-panel ECL port and then on the CAMAC dataway, giving the user two readout options. All zero or zero-and-overflow data words may be suppressed to provide data compression. The front-panel bus system includes the protocol necessary to allow high speed sequential readout to the LeCroy series of ECLine Data Handler Modules and to the Model 4302, Dual Port Fast Memory. The same bus can provide interfacing and data storage in FASTBUS where data can be received by the Model 1892, FASTBUS Memory, or in VME to Memory Model 1190 (request Lecroy application notes AN-4001, AN-4004A and AN-39, and publication P-2 for examples). SPECIFICATIONS ----------
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Model 4418T TDC
Stop lnputs: 8; ECL differential.
Connector: 8x2-pin front-panel connector (Ansley 609-1607). The 8 pins of the left row are positive signal inputs; the 8 pins of the right row are negative signal inputs.
Impedance: 100 ohm differential (50 ohm single-ended on request).
Minimum Width: 10 nsec.
Full Scale Time Range: Normal 200 nsec, corresponding to 50 psec per ADC level. Other values available on request, from 200 nsec to a maximum of 10 µsec.
ADC Resolution: 12 bits.
Integral Linearity: Typically ±0.05% of F.S., better than 0.1% F.S. (measured from channel 200 and 200 nsec of F.S. time range. Higher F.S. time ranges improve proportionally non linearity up to full dynamic).
Differential Linearity: Typically ±0.5%, better than 1%. (Measured from channel 200 and 200 nsec of F.S. time range. Higher F.S. time ranges improve proportionally non linearity up to full dynamic).
Conversion Time: 3 µsec for every valid input channel.
System Busy Time with Zero Suppression: Variable as a function of the number of valid channels.
Valid Channel: 4 µsec.
Channel Without Stop Pulse or Outside the Time Window (LLD-ULD): 1.1 µsec.
Total Busy Time: BTCh 1 + BTCh 2 + ... BT Ch 8 + 1 µsec.
System Busy Time Without Zero Suppression: Fixed 33 µsec.
Time Window: Selected by means of separate lower and upper level discriminators, under CAMAC

control with 8-bit resolution (LLD from 0 to 10%; ULD from 100% to 85%).
DC Offset Control: ±3% of full scale value, under CAMAC control with 8-bit resolution.
Cross Talk Between Two Adjacent Inputs: Maximum ±10% of channel width (±5 psec measured with F.S, time range of 200 nsec).
Full Scale Stability: ±100 ppm/°C.
Zero Stability: ±100 ppm/°C of full scale.

STATUS WORD REGISTER FORMAT
R1-R8 (VSN): Logical address of module: index source for sequential readout with zero suppression.

R10 (SUB): Channel Subaddress Enable (enabled when SUB = 0).
R11 (EEN): ECL Readout Enable. EEN = 1 ECL Readout. EEN = 0 CAMAC Readout.
R12 (OVF): Overflow indication Enable (enabled when OVF = 0).
R13 (CCE): Acquisition and Readout Control.
R14 (CSR):
- With zero suppression (sequential readout) CSR = 1 and CCE = 1.
- Without zero suppression (sequential readout) CSR = 1 and CCE = 0.
- Addressed readout (without zero suppression) CSR = 0 and CCE = X.
R15 (CLE): CAMAC LAM Enable (enabled when CLE = 1). Command Bus
Connector: 8x2-pin front-panel connector. The input matching resistors and output pull-down resistors may be removed to achieve high input and output impedances. When these resistors are mounted, the associated LED indicator (PD ON) is illuminated.
Input Level: Differential ECL.
Impedance: 100 ohm differential.
Output Level: Differential ECL (into 100 ohm differential).
Gate Input (GTE):Gate acts as common start. Pulse width must be time range (200 nsec standard).
Gate Width: 20 nsec to 2 µsec standard, 10 µsec optional.
Clear Input: Common for all analog and digital logic. Pulse width 50 nsec. The module is ready to process a new event after 1.2 µsec.
Request Output (REQ): Indicates that the module is ready to send data to the ECL DATA BUS. The REQ signal is generated at the end of conversion if the bit related to ECL READOUT in the Status Register has been set.
Write Strobe Output (WST): Indicates the time period during which the data present in the ECL Data bus can be stored in the external memory. WST is generated in a minimum of 10 nsec after the data is ready. Its width is higher than 40 nsec. During the entire WST pulse, the ECL Data Bus data is maintained stable.
Write Acknowledge Input (WAK): This input receives the acknowledge signal indicating that the data present on the ECL bus has been loaded into memory and the next data word may be sent. The next WST signal is generated at least 50 nsec after the WAK signal. Minimum WAK width must be 30 nsec.
Busy Output (BSY): This output is set to the "1" state 1 µsec after the end of the GATE signal and is held to this state until after the end of the readout cycle (ECL Readout or CAMAC Readout). The BUSY state may be reset only by sending a CLEAR signal via CAMAC or via ECL BUS (CLR). The ADC is ready to start a new conversion 1.2 µsec after the end of the BUSY state.

ECL PORT ENABLE/PASS
Readout Enable Input (REN): 1x2-pin panel connector. The REN signal indicates to the module that it can take control of the ECL Data Bus; REN must be maintained during the entire readout time. The signal enables the ECL Data Bus, WST Output and WAK input if the module is ready for data transfer (REQ output ON).
Input Level: Differential ECL.
Input Impedance: 100 ohm differential.
Pass Output (PAS): 1x2-pin front-panel connector. Indicates that the module is not ready to transfer data present on the ECL Data Bus or it has finished data transfer. The PASS output signal is generated by the REN line in the absence of the REQ internal command or, if this command is

present, at the end of data readout. The transit time between REN and PASS output is typically 3 nsec if the module does not include data readout capabilities.
Output Level: ECL differential (into 100 ohm differential). ECL PORT OUTPUT
Connector: 17x2-pin front-panel connector (ANSLEY 609-3407). The last two pins are not connected.
Output Level: Differential ECL level (into 100 ohm differential). The pull-down resistors must be removed for high impedance outputs. When these resistors are mounted,the associated LED indicator (PD ON) is illuminated.
Data Word Size: 16 bits.
Readout Mode: Sequential.
Max Readout Frequency: 8 MHz.

CAMAC COMMANDS

CAMAC COMMANDS
Z: Initialize; clears the module and the Status Register.
C: Clears the module; does not clear the Status Register and Memory.
I: Inhibits the front-panel GATE during CAMAC inhibit command.
X: X response is generated for all valid functions.
Q: Q response is generated when the function can be executed.
L: LAM (Look-at-Me) is set after the end of conversion, if it was enabled, with CAMAC Readout enabled.

CAMAC FUNCTION CODES
F(0)·A(0) or F(2)·A(0): Reads Data: a) With zero suppression (CSR = 1 CCE = 1). b) Without zero suppression (CSR = 1 CCE = 0).
Note: CSR and CCE are Status Word Bits (see Status Word).
F(0)·A(0-7) or F(2)·A(0-7): Reads Data: Addressed readout (CSR = 0 CCE = X).
F(0)·A(14) or F(2)·A(14): Reads Header Word.
F(0)·A(15): Reads Pattern Word.
F(2)·A(15): Reads Pattern Word and clears LAM.
F(1)·A(0-7): Reads Threshold Memory (Upper Threshold - ULD).
F(1)·A(8-15): Reads Threshold Memory (Lower Threshold - LLD).
F(4)·A(0-7): Reads Offset Memory.
F(4)·A(9): Reads Common Threshold.
F(4)·A(14): Reads Status Word Register.
Click here for chart
F8·A(0): Tests LAM. Q = 1 if LAM is present.
F9·A(0): Clears the Module.
F10·A(0): Clears LAM and Clears Single Channel Mode.
F17·A(0-7): Writes Threshold Memory (Upper Threshold - ULD).
F17·A(8-15): Writes Threshold Memory (Lower Threshold - LLD).
F20·A(0-7): Writes Offset Memory.
F20·A(14): Writes Status Word.
F25·A(0): Test Function.

READOUT FORMAT

Note: EEN, CSR and CCE are Status Word bits (see Status Word).
1) With zero suppression (sequential readout):
CSR = 1 CCE = 1
EEN = 1 ECL Port Readout
EEN = 0 CAMAC Readout
Click here for diagram

VSN: Virtual Station Number; loaded in the associated Memory.
VDC: Number of Valid Data following Pattern Word (from 1 to 8).
PW: Valid Data View: R1 is referred to Channel 0; R8 is referred to Channel 7.
OVF: Overflow Indication; enabled with OVF = 0 (Status Word bit).
SUB: Channel Subaddress, enabled with SUB = 0 (Status Word bit).
DATA: 12-bit Output Data.
There is sequential readout. CAMAC Readout function F(0)·A(0) or F(2)·A(0).
2) Without zero suppression (sequential readout):
CSR = 1 CCE = 0
EEN = 1 ECL Port Readout
EEN = 0 CAMAC Readout
There is always sequential readout of 8 words.
OVF: Overflow Indication; enabled with OVF = 0 (Status Word bit).
SUB: Channel Subaddress, enabled with SUB = 0 (Status Word bit).
Click here for diagram
3) CAMAC Addressed Readout:
CSR = 0 CCE = Indifferent
EEN = 0 Only CAMAC Readout
There is CAMAC Addressed Readout with F(0)·A(0-7) or F(2)·A(0-7) functions. F(2)·A(7) clears the module during S2. Header can be read out with F(0)·A(14) or F(2)·A(14).
Pattern Word can be readout with F(0)·A(15) or F(2)·A(15).
OVF: Overflow Indication; enabled with OVF = 0 (Status Word bit).
SUB: Channel Subaddress, enabled with SUB = 0 (Status Word bit). Click here for diagram
Simplified block diagram of the Models 4418T.

General
Packaging: RF-shielding 1-width CAMAC module.
Power Requirements: Click here for Table
Note: When all output pull-down and input matching resistors are removed, the current at -6 V is reduced to 1.45 A

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