

Technical Data Evaluation**ITEM: CES-2180 ACC CAMAC Aux. Create Controller (15MHz model)****Evaluation date: 18 November 1985****By: T. Ichihara (RIKEN Radiation Lab.)**

- (1) Hardware CES-2180
- o CPU : DCJ11, 15.0 MHz clock (266.7 n sec clock)
 - o Memory : 64 K bit Static RAM (Hitach HM6246P-12) * 6
128 KB
- (2) Memory bus-cycle
- o Read 1 cycle (0.27 usec) (usec = micro second, hereafter)
 - o Write 2 cycle (0.54 usec)
- (3) Instruction Execution time (by the real measurements)
- (3.1) MOV instruction execution time
(CMP, ADD, SUB are almost identical to MOV)

(*) All the memory reference is on memory (not on I/O page)

(Instruction)	(Exec. time)	MC	Memory Access(*) Fetch/Read/Write		
MOV R0,R1	0.27 usec	1	1	0	0
MOV (R0),R1	0.80 usec	3	1	1	0
MOV (R0)+,R1	0.80 usec	3	1	1	0
MOV @(R0),R1	1.33 usec	5	1	2	0
MOV -(R0),R1	1.07 usec	4	1	1	0
MOV @-(R0),R1	1.60 usec	6	1	2	0
MOV X(R0),R1	1.33 usec	5	2	1	0
MOV @X(R0),R1	1.87 usec	7	2	2	0
MOV #X,R1	0.53 usec	2	2	0	0
MOV @#X,R1	1.07 usec	4	2	1	0
MOV X,R1	1.33 usec	5	2	1	0
MOV @X,R1	1.87 usec	7	2	2	0
MOV R0,(R1)+	1.07 usec	4	1	0	1
MOV R0,@(R1)+	1.60 usec	6	1	1	1
MOV R0,-(R1)	1.33 usec	5	1	0	1
MOV R0,-@(R1)	1.87 usec	7	1	1	1
MOV R0,X(R1)	1.60 usec	6	2	2	1
MOV R0,@X(R1)	2.13 usec	8	2	1	1
MOV R0,#X	2.13 usec	8	2	0	1
MOV R0,@#X	1.33 usec	5	2	0	1
MOV R0,X	1.60 usec	6	2	0	1
MOV R0,@X	2.13 usec	6	2	1	1
MOV (R0)+,(R1)+	1.60 usec	6	1	1	1
MOV -(R0),-(R1)	2.13 usec	8	1	1	1

(3.2) Floating point instruction execution time (by real measurements)

(a) 32bit single precision

(Instruction)	(Exec. time)	Machine Cycle
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(Instruction)	(Exec. time)	Machine Cycle
ADDF FLOAT,0	11.2-13.1 usec	42-49
SUBF FLOAT,0	12.0-14.9 usec	45-55
MULF FLOAT,0	16.3-24.5 usec	61-92
DIVF FLOAT,0	17.1-25.3 usec	64-95

(b) 64bit double precision

(Instruction)	(Exec. time)	Machine Cycle
ADDF FLOAT,0	15.2-17.9 usec	57-67
SUBF FLOAT,0	13.9-18.7 usec	52-70
MULF FLOAT,0	46.4-47.2 usec	174-177
DIVF FLOAT,0	45.1-56.5 usec	169-212

(3.2) Conditional Branch instruction (by real measurements)

1\$:

SOB R1,1\$		
Branch established	1.33 usec	(5 MC)
Branch not established	0.80 usec	(3 MC)

(3.3) Interrupt (calculated value)

(Instruction)	(Exec. time)	Machine Cycle
TRAP	5.33 usec	(20 MC)
RTI	2.40 usec	(9 MC)

(4) CAMAC ACCESS

164000 -165777(O)	CAMAC Address (164000 + 2*A + 64*N)
166000	CAMAC Function Register (CFR)
160002	CAMAC Data High/Status Reg. (DHR)
160004	Interrupt Mask/Source Reg. (IMF)

(4.1) CAMAC READ Cycle Execution Time

(Supposed that the Function is already stored in CFR)

(4.1.1) 16bit, Read into a register (R5 shows CAMAC address)

MOV (R5), R0 1.46 usec (10 clock stretched read)

(4.1.2) 16bit, Read into a memory (R5 shows CAMAC address)

MOV (R5), (R1)+ 2.27 usec (10 clock stretched read)

(4.1.3) 24bit, Read into a memory (R4 shows SHR)

MOV (R5), (R1)+ 2.27 usec (10 clock stretched read)
MOV (R5), R0 1.87 usec (10 clock stretched read)-----
total 4.13 usec

(4.1.4) 16-bit address scan block-mode read I (SOB loop)

1\$: MOV (R5)+, (R1)+ 2.27 usec
SOB R0,1\$ 1.33 usec-----
total 3.60 usec / 1 word read (550 kB/sec)

(4.1.5) 16-bit address scan block-mode read I (MACRO expansion)

.REPT n

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MOV (R5)+, (R1)+    2.27 usec  
.ENDM
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2.27 usec / 1 word read (882 kB/sec)

(4.2) CAMAC WRITE Cycle Execution Time

(4.2.1) 16-bit write from register

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MOV R0, (R5)    1.33 usec (8 clock stretched write)
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(4.2.1) 16-bit write from memory

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MOV (R1)+, (R5) 1.87 usec ( 1.07 MB/sec)
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(5) test interrupt program execution time

In the interrupt routine

- (1) Push registers
- (2) read 8 CH CAMAC Data into Memory
- (3) Write Output register 2 words (pulse)
- (4) pop registers

Time from the interrupt to the pulse of the Output register

20 instructions: 38.42 usec

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