CLOSY3
Clock Synthesizer IIIrd

Project kick-off

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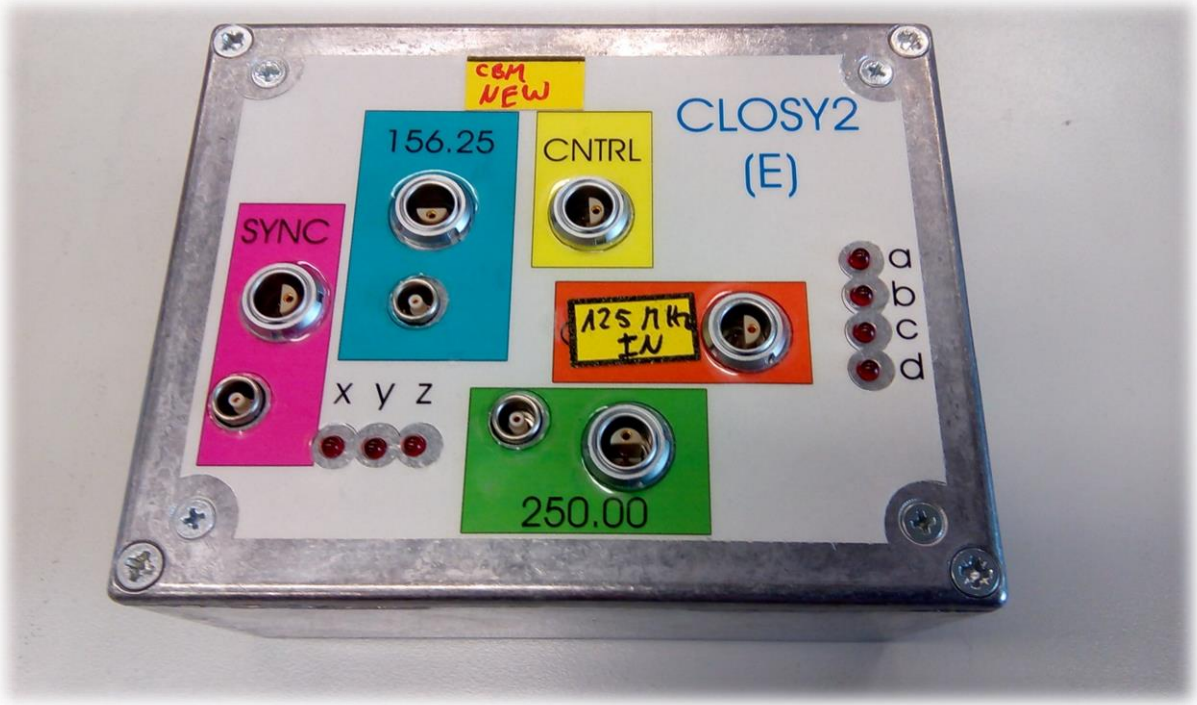
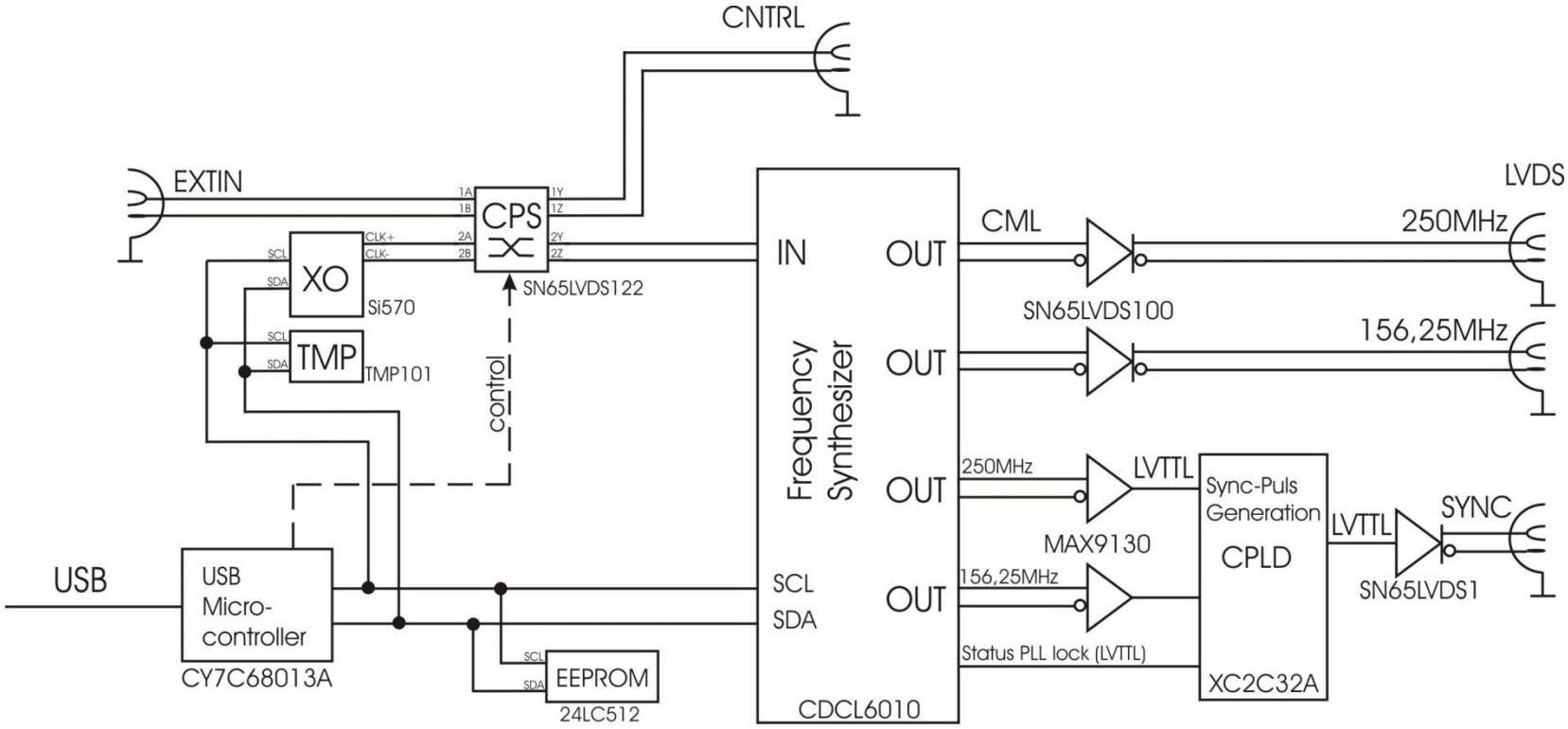
Outline

- Scope of the project
- Introducing the AD9516 clock synthesizer
- Introducing the CLOSY3
- Synchronizing campus-wide
- Project planning
- Conclusions
- Questions

The CLOSY we all know and love



The CLOSY we all know and love



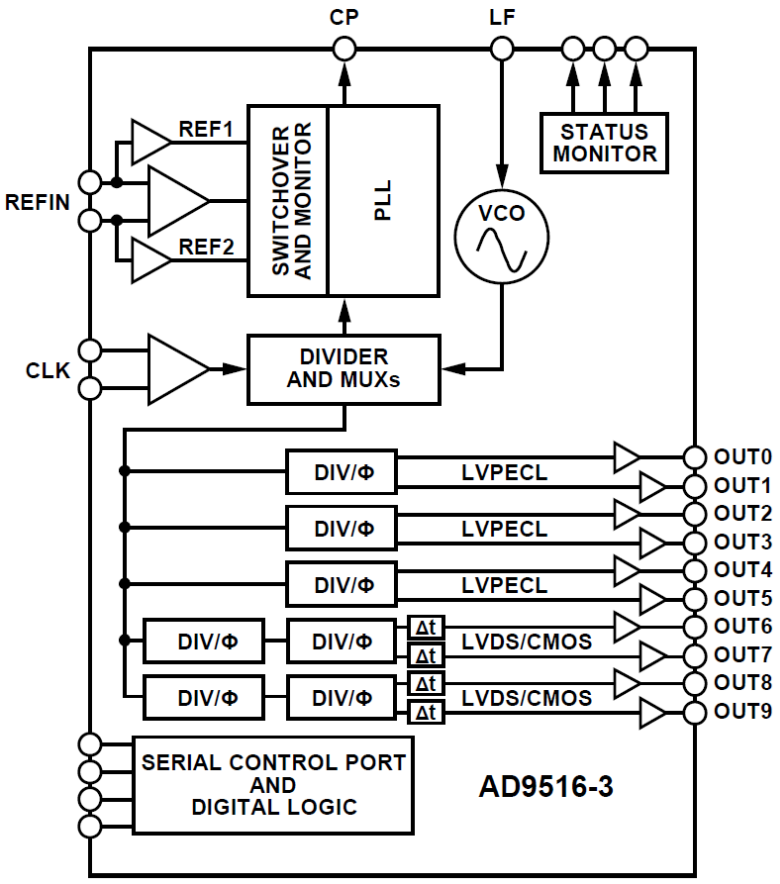
So why do we need a new CLOSY?

- Synchronization to campus-wide GMT/BuTiS
- Applications
  - Generate variable frequencies in the lab (ADCs/DACs/etc.)
  - Clock distribution
  - CBM ToF (replace the CLOSY2)
  - Separation between two WR-based timing networks
  - [...]

and finally...

- I need a h/w project to start on at GSI ☺

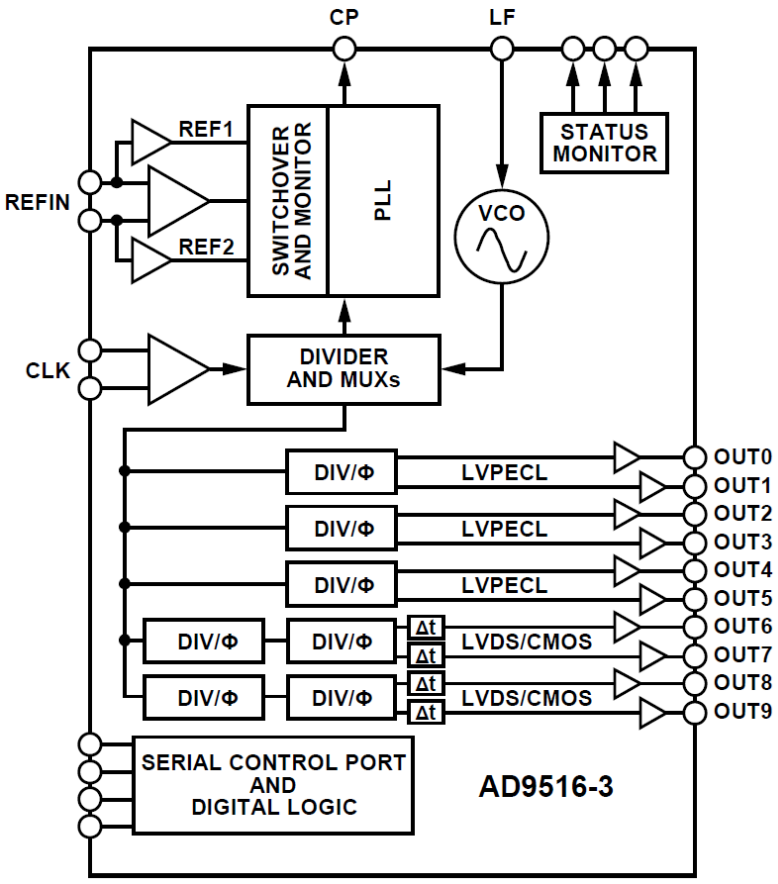
A very cool clock synthesizer chip...

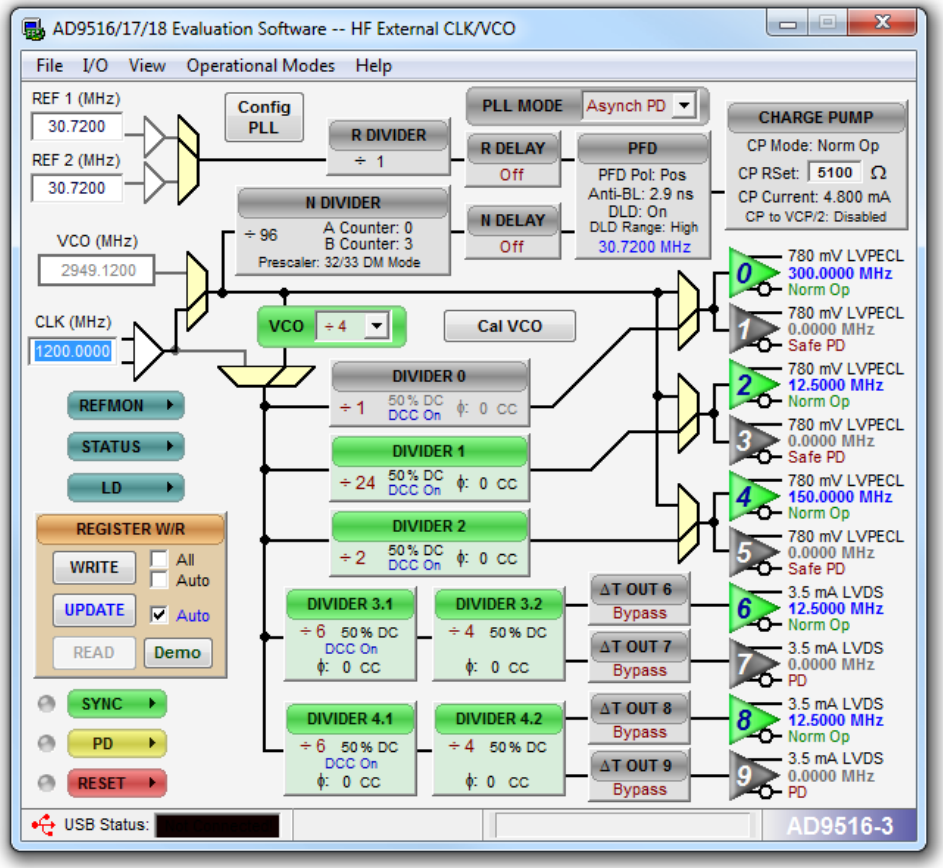


- On-chip PLL (only external loop filter required)
- On-chip VCO (1.75-2.25 GHz)
- LVPECL outputs up to 2.9 GHz (but needs 2.9 GHz CLK input)
- LVDS outputs up to 800 MHz
- CMOS outputs up to 250 MHz
- Control via SPI

and...

… with its own PC software

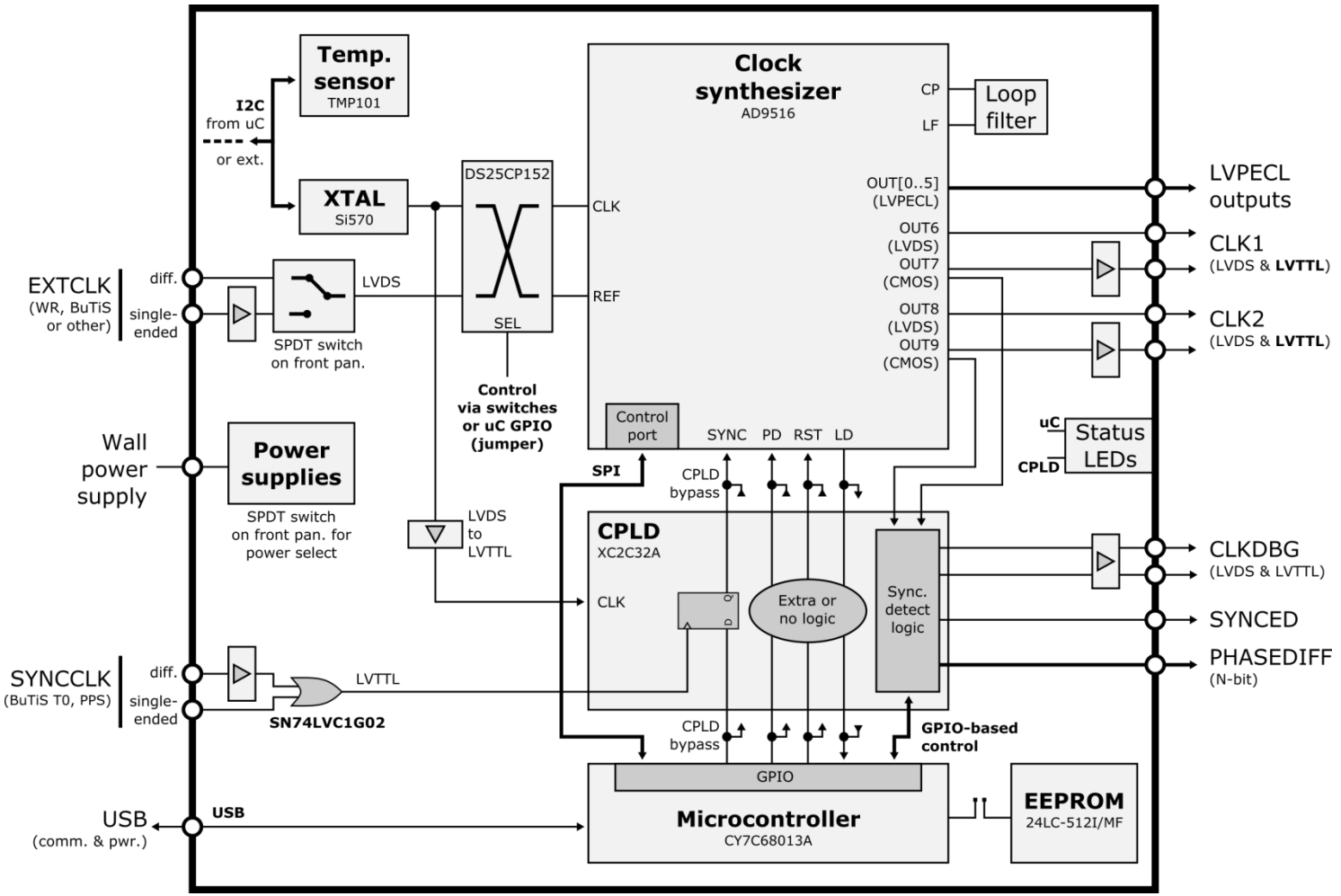




So, the plan is:

- Use the AD9516-3 instead of the CDCL6010
- Generate a configuration for the AD9516-3 via its software
- Download the data to an on-board microcontroller
- The microcontroller downloads the clock configuration data to the chip

Presenting... the CLOSY3

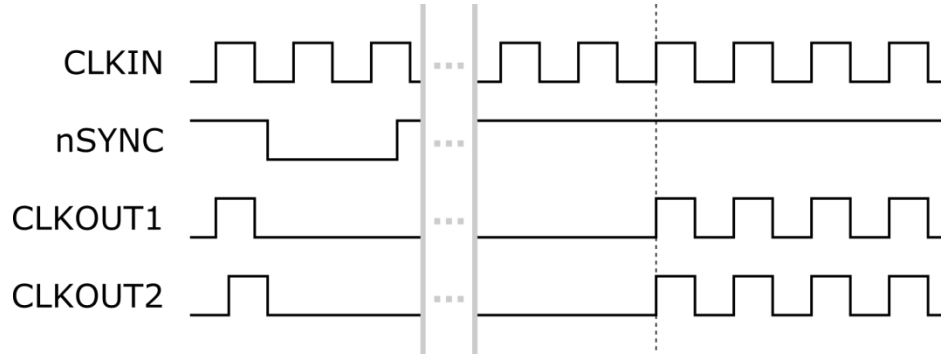


Design concepts

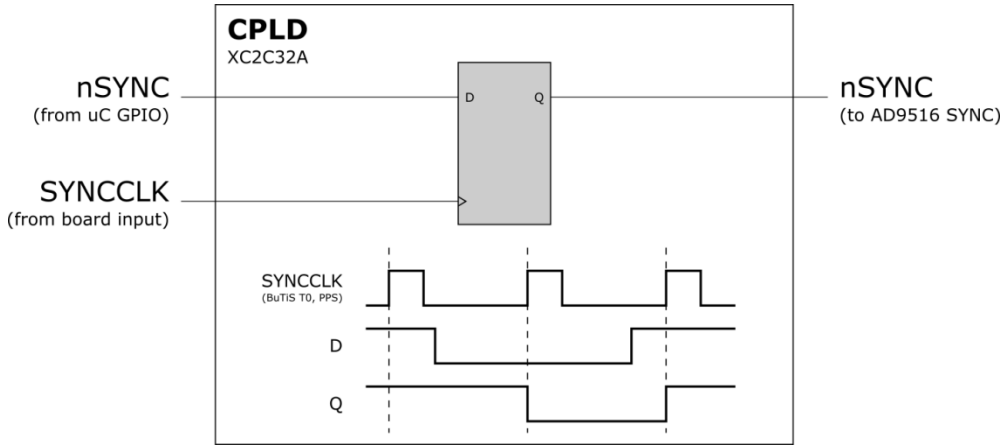
- Re-use as much as possible
- CY7C68013A microcontroller is already used
  - on AD9516-3 eval. board
  - on the CLOSY2
  - on timing receivers
- Crossbar switch
  - selects between external or on-board clock (from Si570 clock synthesizer – up to 1.4GHz)
  - clock(s) can be input to the AD9516-3 in any way to either the CLK or PLL REF inputs
- Power from either wall PS or USB
- TMP101 for temperature measurements
- CPLD for synchronization

Implementing campus-wide sync.

- Synchronizing two clocks with the same freq. using the AD9516-3



- We can sync clocks campus wide using a simple FF inside the CPLD



Planning, planning, planning...

- adding components to database	1 wk.
- schematics design	3 wks.
[- schematics review]	
[- component order here]	
[- software design for Cypress uC]	
- layout	4 wks.
[-layout review]	
- schematics + layout review	1 wk.
- production	8 wks.
- assembly	2 wks.
- test & debug	4 wks.
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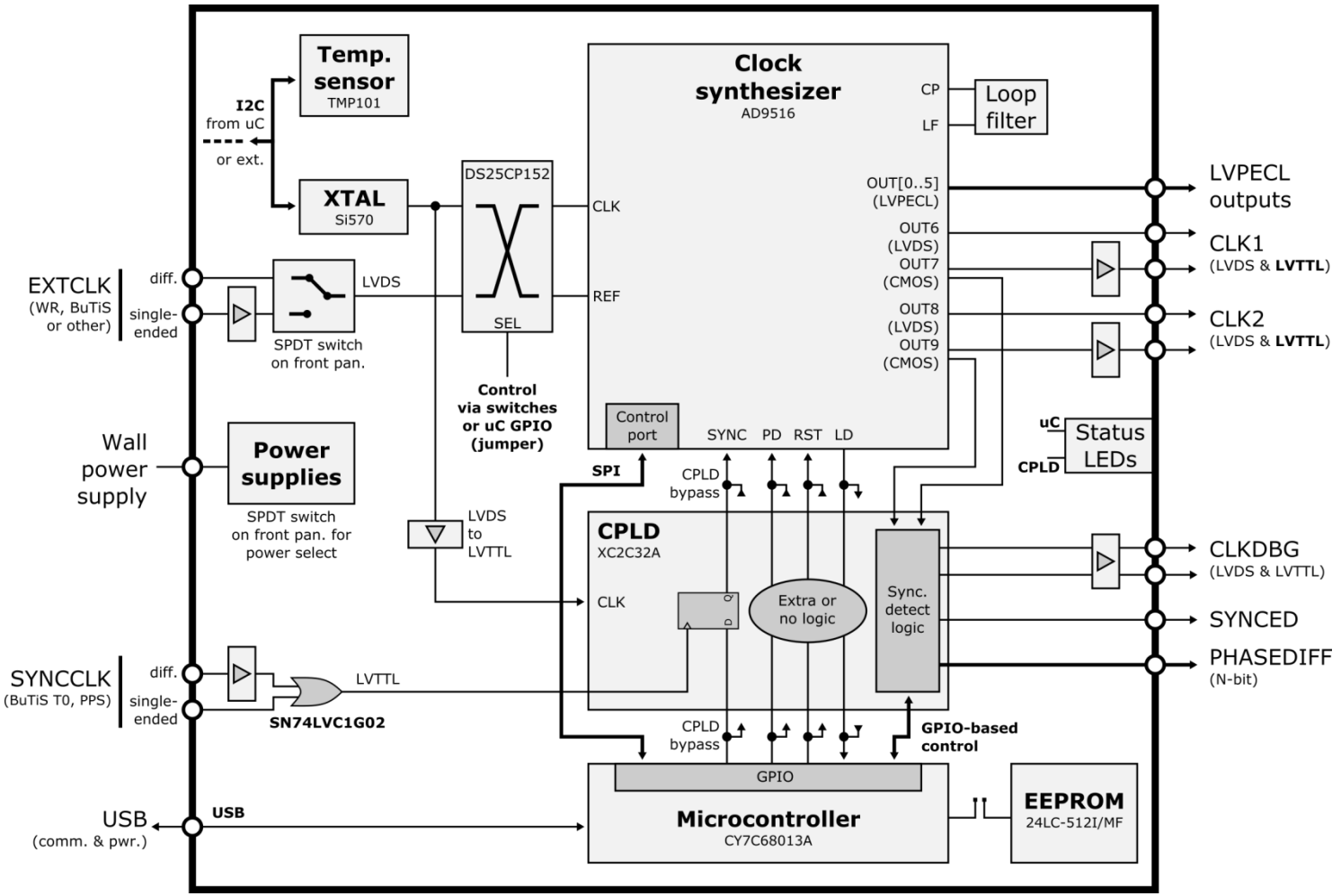
	23 wks.

Done by beginning of November 2015 (starting in W22).

extra things for planning, going on in parallel with previous

Kick-off!


Temp. sensor
TMP101
I2C
from uC
or ext.
XTAL
Si570
DS25CP152
CLK
REF
SEL
Control via switches or uC GPIO (jumper)
Clock synthesizer
AD9516
CP
LF
Loop filter
OUT[0..5] (LVPECL)
OUT6 (LVDS)
OUT7 (CMOS)
OUT8 (LVDS)
OUT9 (CMOS)
LVPECL outputs
CLK1 (LVDS & LVTTL)
CLK2 (LVDS & LVTTL)
EXTCLK
(WR, BuTiS or other)
diff.
single-ended
LVDS
SPDT switch on front pan.
Wall power supply
Power supplies
SPDT switch on front pan. for power select
Control port
SYNC
PD
RST
LD
SPI
CPLD bypass
uC
CPLD
Status LEDs
LVDS to LVTTL
CPLD
XC2C32A
CLK
Extra or no logic
Sync. detect logic
CLKDBG
(LVDS & LVTTL)
SYNCED
PHASEDIFF
(N-bit)
SYNCCLK
(BuTiS T0, PPS)
diff.
single-ended
LVTTL
SN74LVC1G02
GPIO-based control
GPIO
USB
(comm. & pwr.)
USB
Microcontroller
CY7C68013A
EEPROM
24LC-512I/MF

Questions?

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