

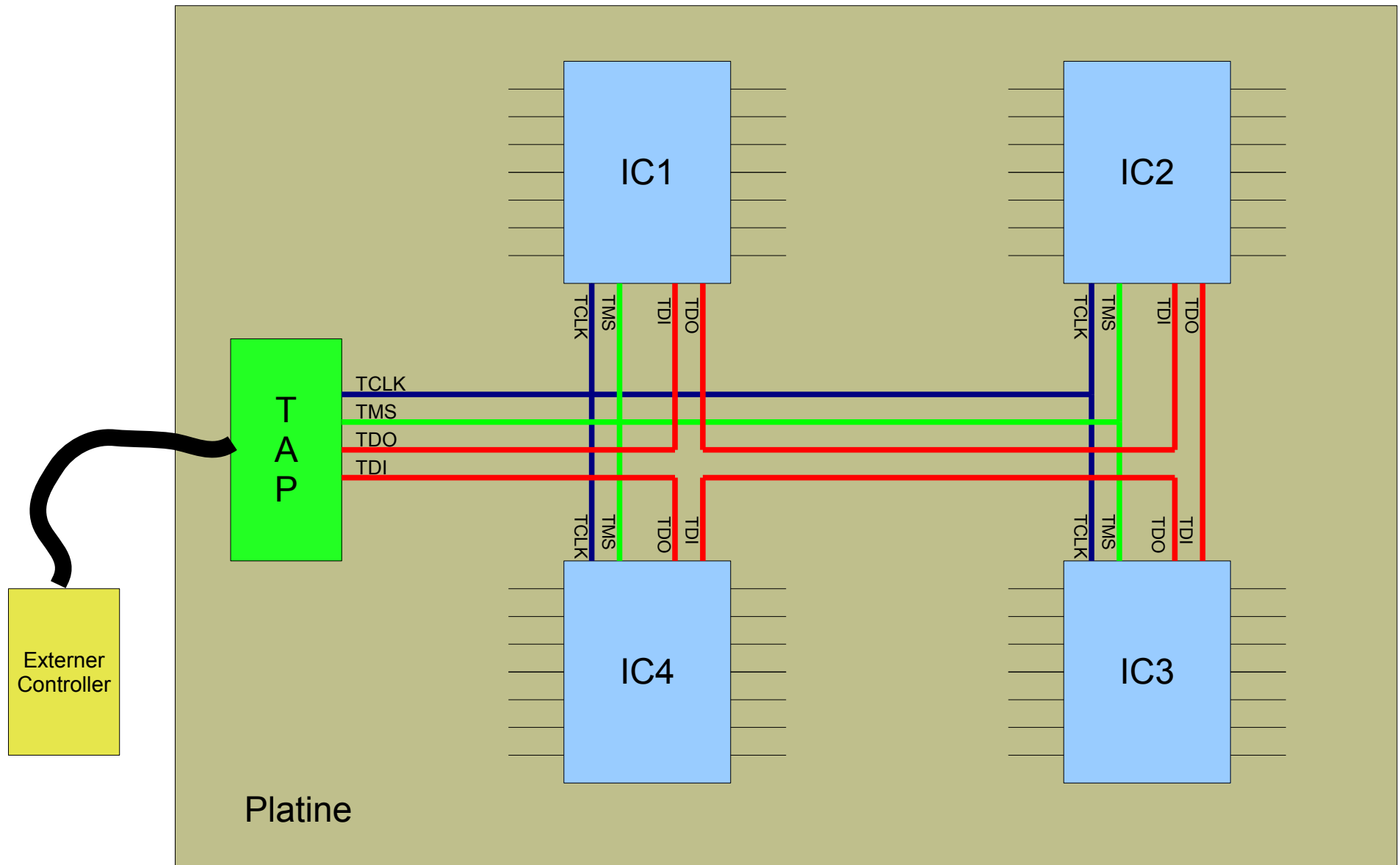
# JTAG – IEEE 1149.1

- Problem
  - Testbarkeit von Platinen und ICs
- JTAG = Joint Test Action Group
  - 1985 (Philips, TI, AT&T, IBM, ...)
- Ziel:
  - Definition neuer Testmethoden für ICs und Platinen
- Ergebnis:
  - 1990: Boundary Scan Test angenommen als IEEE1149.1

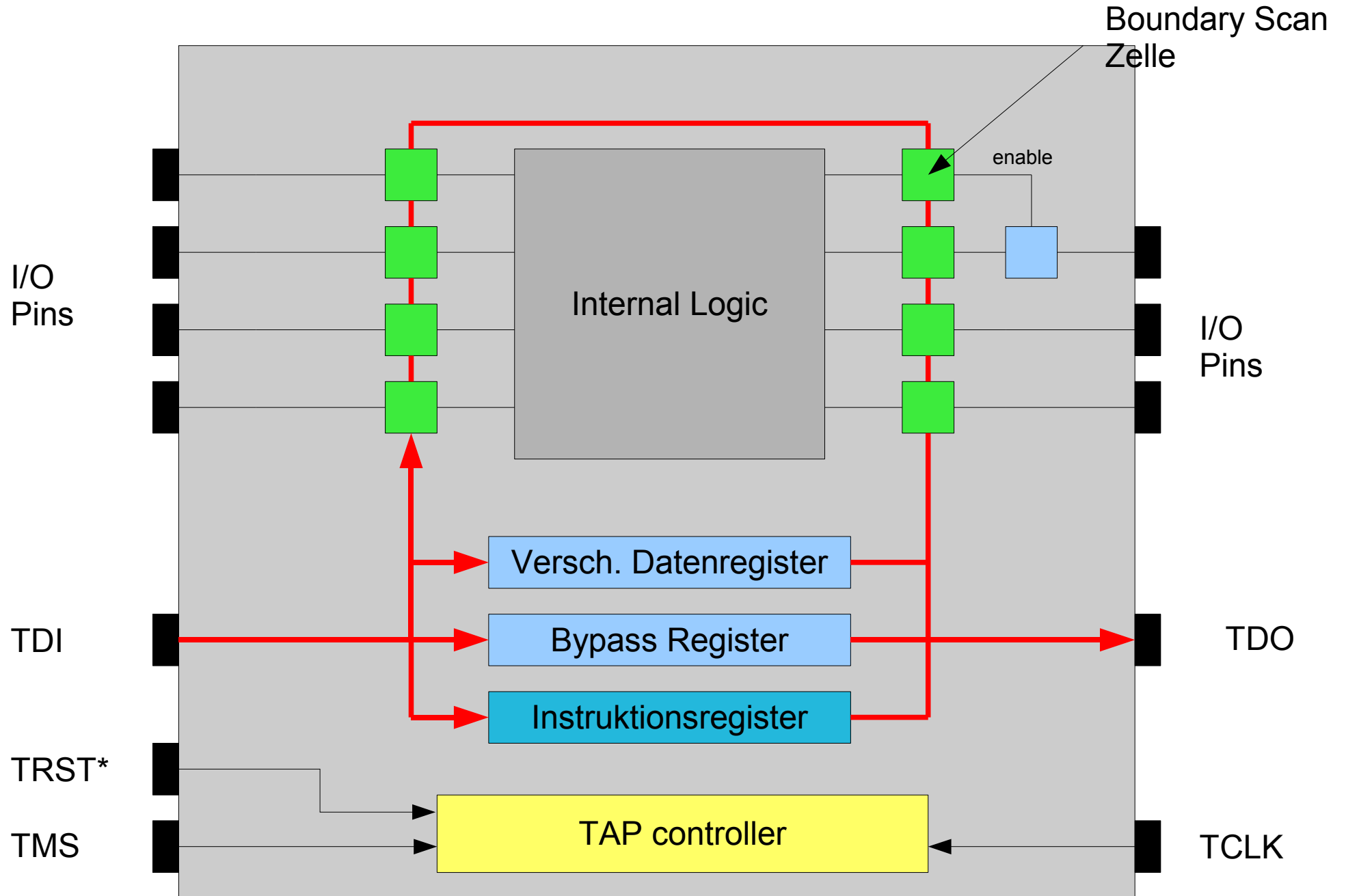
# Boundary Scan

- Grundidee:
  - Jeder IC hat 4 wesentliche Hardwareelemente:
    - Test Access Port (TAP)
    - TAP Controller
    - Instruktionsregister
    - Mehrere Datenregister
  - BSDL (Boundary Scan Description Language)
    - Subset von VHDL, beschreibt Boundary Scan Eigenschaften
- Test Access Port (TAP)
  - 4(5) Pins:
    - TDI: Test Data in
    - TDO: Test Data out
    - TCK: Test Clock
    - TMS: Test Mode Select
    - TRST: Test Reset (optional)

# Boundary Scan



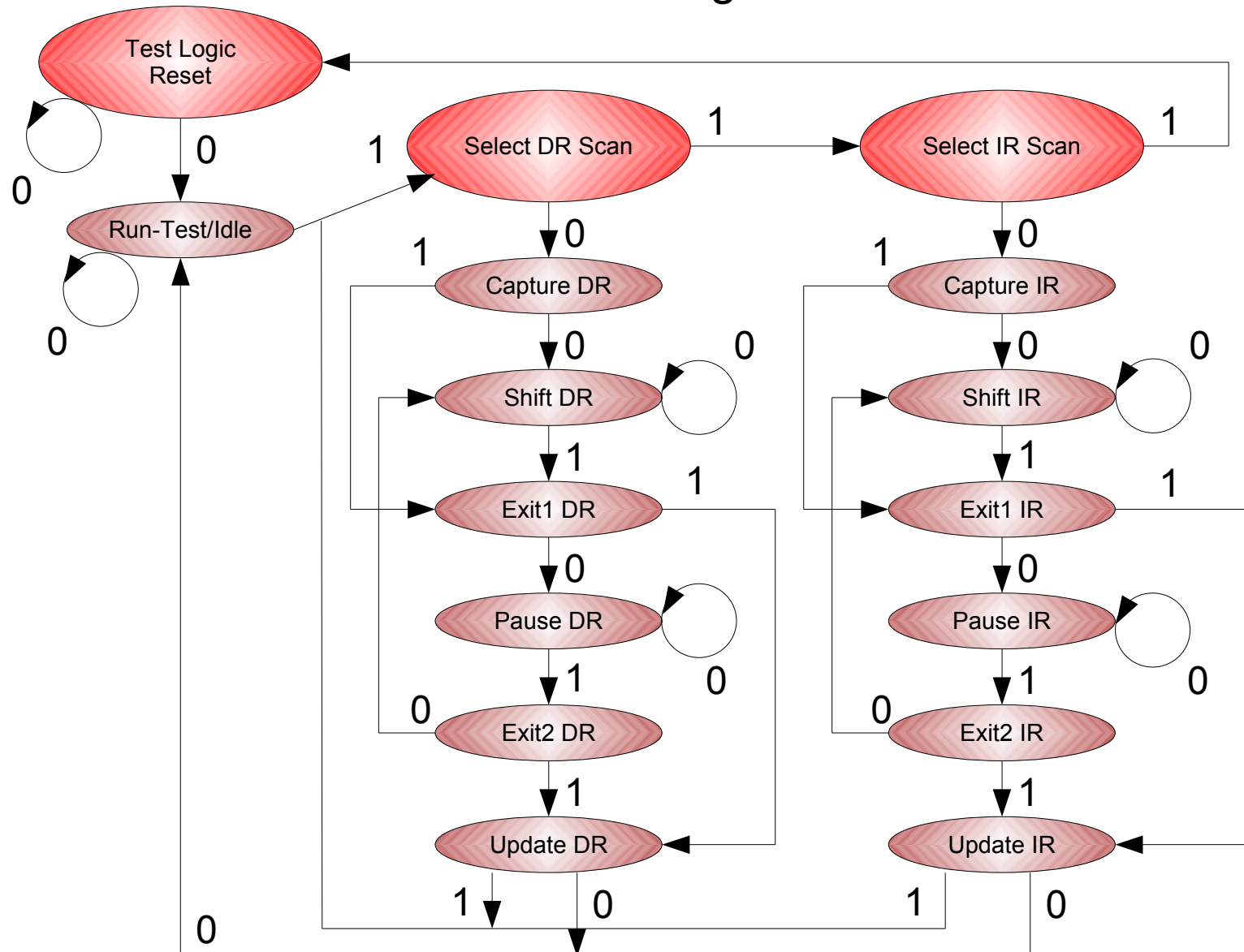
# IC mit Test Controller und Boundary Scan Registern



# • TAP Controller

- gesteuert durch TMS Signal

## State Diagramm des TAP Controllers



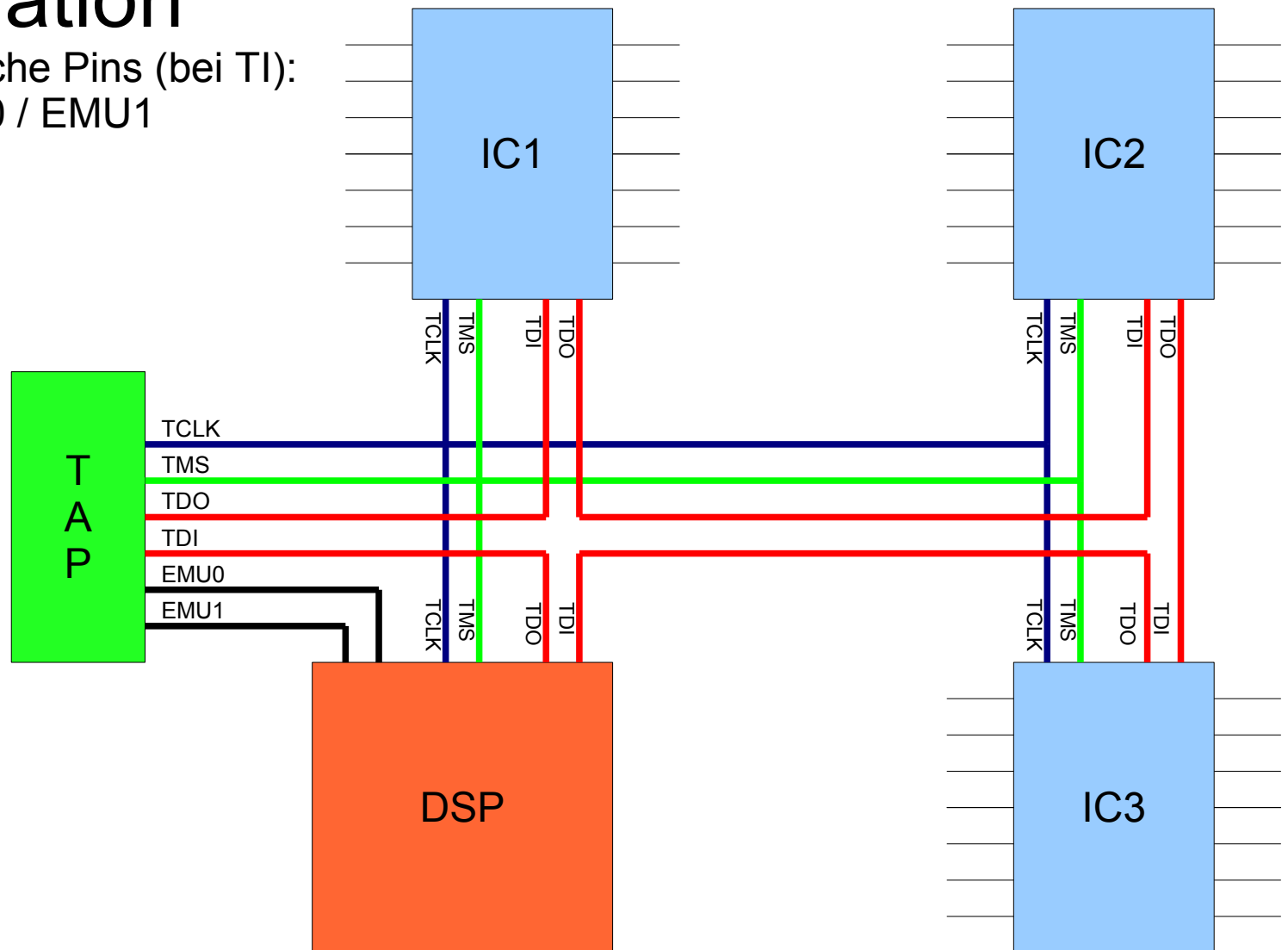
# Boundary Scan

- Instruktionsregister IR
  - Instruktionen:
    - obligatorisch:
      - Bypass, Sample/Preload, Exttest
    - optional:
      - Intest, Runbist, Clamp, ...
    - Herstellerspezifisch
      - private Instruktionen für Spezialanwendungen
- Datenregister
  - Boundary Scan Register
  - Bypass Register
  - Device ID Register
  - Designspezifische Register

# Spezielle Anwendungen

- Emulation

- 2 zusätzliche Pins (bei TI):
  - EMU0 / EMU1







# Boundary Scan bei ELEX

## Since 1995 used Functions

1. Test of Printed Board, (SAM2)
2. DSP Emulation, (C40....C6000)
3. CPLD In Circuit Configuration.
4. Other.

# Software

ASSET for PCB tests.

Code Composer for DSP emulation.

MAX+2: CPLD, FPGA. (ISP used since 1995).

PHILIPS: CPLDs. since 1998.

XILINX: FPGAs, CPLDs since 2001.

BSD files.

JTAG chain description.

# Hardware

PCB with BS devices, path and connectors.

Emulator Interface.

Parallel or USB cable adapter for ISP.

# BSD Devices

CPLDs

FPGAs

DSPs

LOGIC

TDCs

others

# Problems

Chain debugging.

I/O common with JTAG pins.

FPGA in false mode.

Signal integrity.