ECP5 SERDES issues

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Outline

Specs of Lattice ECP5

- 4 SERDES channels
- Up to 5 Gb/s (ECP5-5G) or 3.2Gb/s (ECP5)
- 17 application notes + datasheet
- SERDES application note: 100 pages
- 300 registers to configure

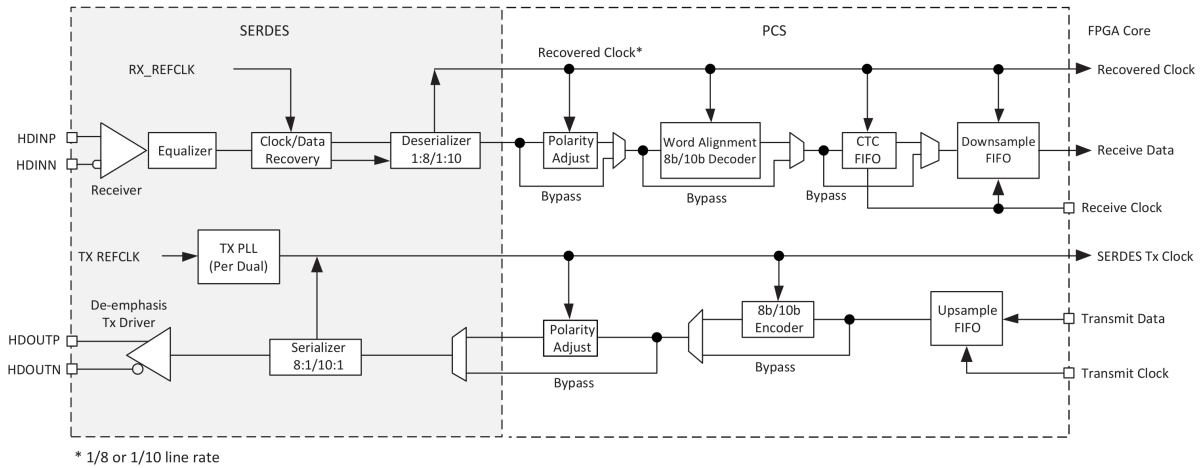


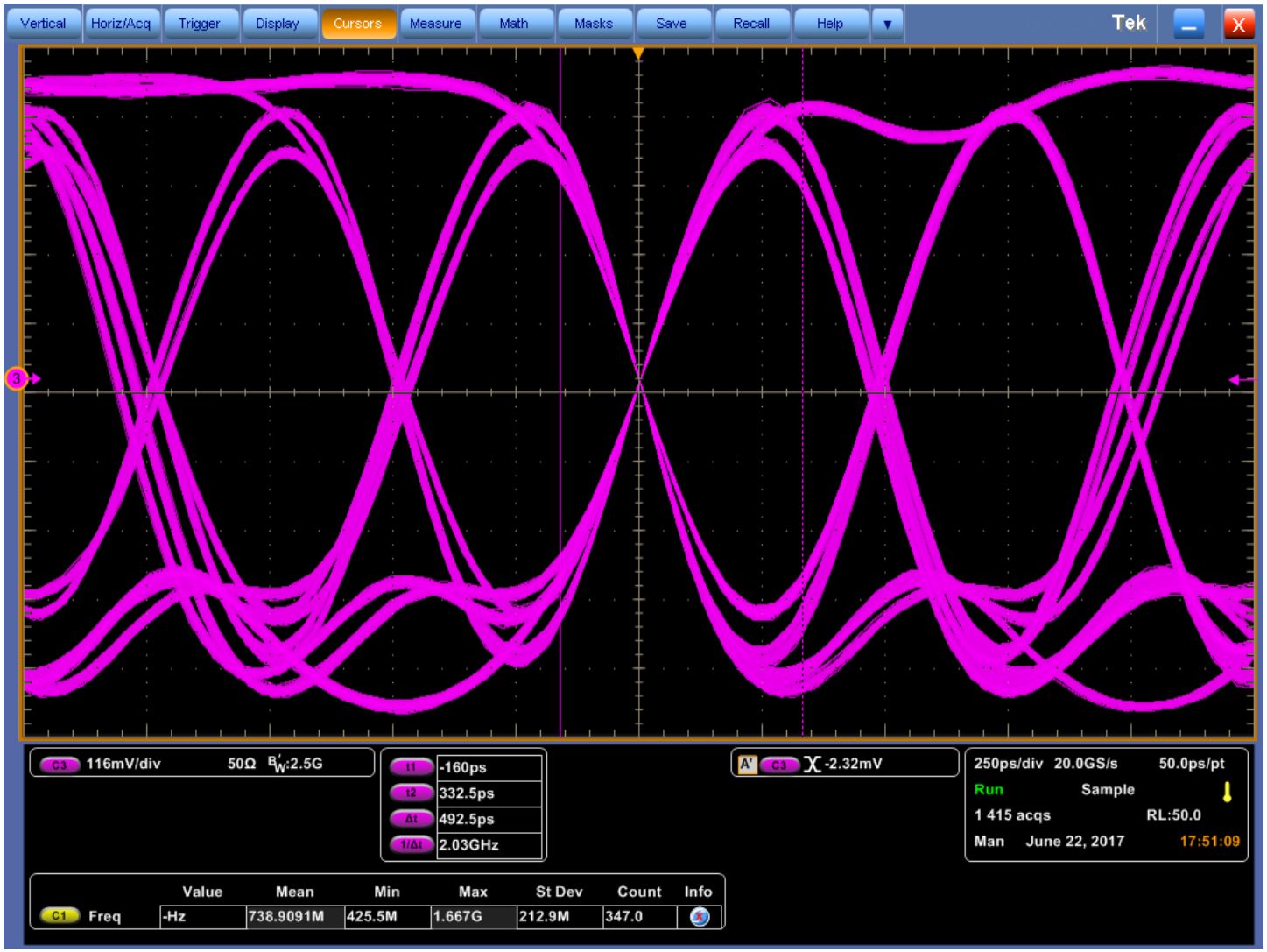
Figure 2.28. Simplified Channel Block Diagram for SERDES/PCS Block

Operation of larger systems at nominal voltage

- for normal parameters (+- 1500ppm for loss of lock)
  - 1/3 of 30 DiRICH were working
- with more tolerance (+-7000ppm)
  - 2/3 of the DiRICH were working
- with additional reduced voltage of Vcc (nominal 1.1V)
  - 4/5 of the DiRICH were working
  - done measurement with this, but shaky system

- Checking all details of schematics, datasheet, application notes, layout and at the end measure all inputs and outputs

Eye-Diagram of RX Differential Input



SERDES Supply

- After quite some struggeling and tests
- SERDES needs 6 separate Voltages
  - Vcc, VccHRX und VccHTX, VccA, VccAux, VccAuxA
  - default: all to 1.1V or 2.5V
- All supply voltages are "immune" to small changes (+-100mV)
- except VccA
- Operating from 0.95V to 1.05V
  - all fine!
  - Above 1.06V PLL lock is lost
  - sideremark: For higher frequencies it works better
- Fix: BLM15- instead of BLM18-
  - series resistance: 1.1Ohm instead of 0.3Ohm
    - results in 70mV drop